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Design and Simulation of a Multistages Common-Emitter, Common-Collector, AC Voltage Amplifier

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A B S T R A C T

The main function of the ampifier is to increase the signal strength, in terms of its voltage or current. In this research, a multistages ac voltage common-emitter amplifer and common-collector amplifier with a single supply of +15 V was designed. The objective is to design an amplifier for amplifying a small ac signal from a transducer. The transducer has an output impedance of 10 kΩ. The amplifier will have a small-signal gain in order of about 1500 and a small-signal bandwith ranging from 100 Hz to 20 kHz. It will drive a load of 300 Ω. The entire circuit consists of a first stage common-emitter configuration gain amplifier, another second stage common-emitter configuration gain amplifier, and a third stage buffer unity gain common collector amplifier. The three-stages was capacitor coupled. The overall gain of the entire amplifier is the product of the first-stage gain, the second-stage gain, and the third-stage gain. A method called short-circuit time constants was used to determine the apropriate coupling and bypass capacitors. The overall circuit was then simulated by using NI Multisim. The magnitude of the overall gain of the circuit was obtained by performing an interactive analysis and simulation. The frequency response of the amplifier was obtained by performing an AC sweep analyses and simulation. It can be showed that the amplifier's overall gain obtained from simulation is in agreement with the calculated results. The simulated result for the frequency responses were also in agreement with the requirement

INTRODUCTION

An amplifier is a device for increasing the power of a signal. This is accomplished by taking energy from a power supply and controlling the output to duplicate the shape of the input signal but with a larger (voltage or current) amplitude. In this sense, an amplifier may be thought of as modulating the voltage or current of the power supply to produce its output [1].

The use of amplifiers in electronic products is very important. The main function of the ampifier is to increase the signal strength. In other words, the amplifier will make the output signal larger in magnitude than the input signal. A practical example is in the radio or television. The radio or television signal received by an antena is so weak that it cannot adequately drive a loudspeaker or television tube. This weak signal need to be increased, or amplified until it has enough power to be useful. This increase in amplitude (amplification) is called the gain of the amplifier.

In many practical applications, a single amplifier cannot serve all the gain that is required to drive a particular kind of load. For example, in a speaker that represents a "heavy" load in an audio amplifier system. Several amplifier *stages* may be required to "boost" a signal originating at a microphone or magnetic tape head to a level sufficient to provide a large amount of power to the speaker. We also have heard components such as *preamplifiers*, *power amplifiers*, and *ouput amplifiers*, all of which include stages of amplification in their system. Actually, each of these components may itself consists of a number of individual transistor amplifier stages. Amplifiers that generate voltage, current, and/or power gain through the use two or more stages are called *multistages* amplifier [2].

Thus, practical transistor amplifiers usually comprises of a number of stages linked in cascade. The first stage of a multistages is for providing a gain. Other than providing the gain, the first (or input) stage is usually utilised to provide with a high input resistance so that loss of signal level can be avoided when the amplifier is fed from a high-resistance source.

The middle stage function's is to provide with the bulk of the voltage gain. Besides that, it provides with other functions such as the conversion of the signal from differential mode to single-ended mode

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The last stage is an amplifier that has a voltage gain of only unity. This amplifier has a very high input resistance, thus almost all of signal source voltage will appear at the input of the amplifier proper. Since this amplifier has a low output resistance, 90% of this signal will appear at the output

In this multistages amplifiers, the output of previous stage is linked to the input of next stage using a coupling device. A capacitor or a transformer can usually be used as the coupling device. The process of connecting two amplifier stages using a coupling device is called cascading [4]. In other word, when the output of one amplifier stage is connected to the input of another next stage, the amplifier stages are said to be in *cascade*. The following Fig. 1 shows the block diagram of a three-stage amplifier connected in cascade

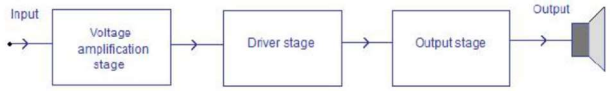

Figure 1. A Three-Stage Amplifier Connected in Cascade

The overall gain is the product of voltage gain of individual stages, i.e. $G_{overall} = A_{V1} \times A_{V2} \times A_{V3} = \frac{V_2}{V_1} \times \frac{V_3}{V_2} x \frac{V_o}{V_3} = \frac{V_o}{V_1}$. Where $G_{overall} =$ overall gain, $A_{v1} =$ voltage gain of 1^{st} stage, $A_{v2} =$ voltage gain of 2^{nd} stage, and $A_{V3} =$ voltage gain of 3^{rd} stage.

Some research about designing a multistage amplifier can be mentioned as follows. First, there is a research conducted by J. Vuolevi and T. Rahkonen [4] discussing about the important role of source impedance in minimizing the distortion of a common-emitter BJT-stage. Another research by Xiao-Hong Wu, Bin Wu, Jun Sun, and Zhen-Yu Wang [5] titled *Simulation and Analysis of the Common-Emitter Circuit in Analog Electronics Teaching* discussing the importance of NI Multisim as an Electronics Design Automation (EDA) tool for designing, analysing, and simulating a common-emitter configuration amplifier. Another research done by Risa S. Assaad and Jose Silva-Martinez [6] titled *A Graphical Approach to Teaching Amplifier Design at the Undergraduate Level* proposes a novel graphical approach which presents the complete amplifier design in a visual form that is easy for the students to understand. with design of a bipolar junction transistor common-emitter (BJT-CE) amplifier is used as an illustration. A research performed by Dan Dan-Abia, Akaninyene Obot, and Kufre Udofia [7] titled *Design and Analysis of a Multistage Common Emitter Amplifier for Low Frequency Applications* presents a multistages common-emitter amplifier simulated with LT SPICE. A research done by H. Babaie [8] titled *A technique to stabilize the output voltage level of an emitter follower* discussed about an emitter follower configuration. Then, D. L. Rode [9] with his research titled *Output resistance of the common-emitter amplifier*, presents about the independency of the output resistance of the common-emitter (CE) amplifier from its signal-source resistance

A research done by I. M. Pandiev and E. C. Stoimenov [10] developed a low-power multistage amplifier laboratory kit for engineering education. The laboratory kit contains a multistage amplifier built by the basic transistor stages used in operational amplifiers. Each stage is implemented with discrete components. The key functional blocks of the circuit are a differential amplifier as an input stage, followed by a common-collector amplifier as a buffer and an output stage. The same authors also proposed a research [11] titled *Development of Single-Transistor Amplifier Modular Laboratory Kits for Electronic Engineering Education* which develop two laboratory kits containing two single-stage amplifier circuits that are constructed using discrete components. The object of study is the AC behavior of the two basic amplifier configurations with single BJT and MOSFET.

In this research, a three-stage AC voltage amplifier were designed. The purpose of the research is to design a multistages ac voltage amplifier that has capabilty to amplify ac signals from a transducer. The transducer has an output impedance of 10 kΩ. This amplifier will have a small-signal gain of about 1500, and a small-signal bandwidth from 100 Hz up to 20 KHz. This amplifier will have an output signal with a peak-to-peak not less than 8 Volt when driving load of $300\ \Omega$.

The overall amplifier design was consisted of a first stage common-emitter configuration, a second stage common-emitter configuration, and a third stage buffer unity gain common-collector (emitter follower) configuration.

The quantities of common interest about an amplifier are its amplification (or gain) and its input and output resistances. For single-input, single-output circuits, several kinds of incremental gain are of interest: power gain, voltage gain, current gain, transconductance, and transresistance [12]. In this research, the quantities that of our interest for our amplifier are the amplifier's voltage gain, its input resistances and output resistances. Thus, in this article, lots of calculations will be encountered for calculating those three parameters

This article was written with the following order. First, an explanation for the common emitter configuration with its biasing which form the common-emitter amplifier was introduced. The design process of the first stage and the second stage of this multistages amplifier was then carried out. Next, an explanation for the emitter follower configuration with its biasing which form the emitter follower amplifier was introduced, which followed by its design process. Finally, the process of determining the value of coupling and bypass capacitors for the frequency response was presented.

COMMON EMITTER CONFIGURATION

Figure. 2 below shows a transistor circuit where the emitter terminal is connected to ground, the input voltage signal v_i is taken between the base and ground, and the output voltage signal v_o is applied between the collector and ground, across the resistance R_C. Due to the conection from the emitter terminal to ground, this configuration is called the grounded-emitter or common-emitter (CE) amplifier.

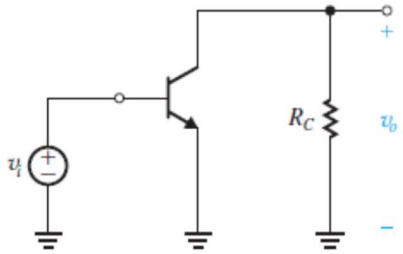

Figure 2. A Common-Emitter Configuration

THE CLASSICAL DISCRETE-CIRCUIT BIAS ARRANGEMENT

An important step in the design of a transistor amplifier is the establishment of an appropriate dc operating point for the transistor. This step is known as biasing or bias design. The bipolar transistor will function most linearly when confined to operate in the forward-active region. The dc operating point therefore must be selected so that the transistor remains in the forward-active region at all times for which a time-varying signal is superimposed on quiescent levels. Distortion of the output signal results if an operation point is chosen that causes the BJT to be saturated or cut off (or both) when a signal is applied [13].

Fig. 3 shows the arrangement most commonly used for biasing a discrete-circuit transistor amplifier if a single power supply (shown as V_{CC}) is used. The technique is performed by supplying the base of the transistor with a fraction of the supply voltage V_{CC} through the voltage divider R_1, R_2. In addition, a resistor R_E is connected to the emitter. The design considers the finite base current.

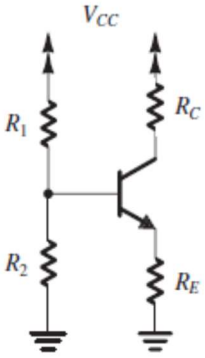

Figure 3. A Single Power Supply for Classical Biasing of BJTs

Next, Fig. 4 shows the equivalent circuit of Fig. 3, but this time with the voltage-divider network substituted with its Thévenin equivalent,

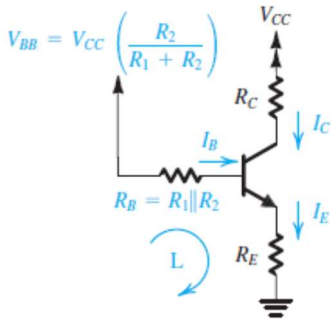

Figure 4. Circuit of Fig. 3 with Its Thévenin Equivalent Version.

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \quad (1)$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \quad (2)$$

The current I_E can be calculated by applying a Kirchhoff loop equation for the base–emitter–ground loop, labeled L, and substituting $I_B = \frac{I_E}{(\beta + 1)}$:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + \frac{R_B}{(\beta + 1)}} \quad (3)$$

To make I_E insensitive to temperature and β variation, we design the circuit to conform with the following two constraints:

$$V_{BB} \gg V_{BE} \quad (4)$$

$$R_E \gg \frac{R_B}{(\beta + 1)} \quad (5)$$

It should be noted that condition in equation (4) ensures that small variations in V_{BE} ($\cong 0.7\ V$) will be overruned by the much larger V_{BB}. And condition in equation (5) makes I_E insensitive to variations in β and could be satisfied by selecting R_B small. This in turn is achieved by using low values for R_1 and R_2. Lower values for R_1 and R_2, however, will mean a higher current drain from the power supply. This will lower the input resistance of the amplifier (if the input signal is coupled to the base, as will be done in this design). This is the trade-off involved in this part of the design. It should be noted that condition in equation (5) means that we want to make the base voltage independent of the value of β and determined solely by the voltage divider. This will obviously be satisfied if the current in the divider is made much larger than the base current. Typically one selects R_1 and R_2 such that their current is in the range of I_E to $0.1I_E$.

A COMMON-EMITTER AMPLIFIER

The common-emitter (CE) amplifier is the most widely used of all BJT amplifier configurations. This is because of its high efficiency and positive gain greater than unity [14].

Fig. 5 shows a CE amplifier with the classical biasing arrangement of Fig. 3. It makes use of coupling capacitors C_{C1}

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and C_{C2} and bypass capacitor C_E. Here we assume that these capacitors, while at the same time blocking dc signal, they behave as perfect short circuits at all signal frequencies of interest [15].

We will explain about the significance of this coupling capacitors. In many amplifier applications, the source or the load, or both, cannot be subjected to a dc voltage or be permitted to conduct a current. For example, an electromagnetic speaker is design to respond to ac fluctuations only and may not operate properly if it conducts a dc current. To overcome this, a capacitor is connected in series with the load to prevent the dc component of an amplifier's output voltage from producing dc current in the load. Similarly, a capacitor is connected in series with the source to prevent the flow of dc current from the amplifier into the signal source (or vice versa). The capacitors are called *coupling* capacitor, or *blocking* capacitor, since they block the flow of dc current. In order to present negligible impedance to the ac signals, the capacitors chosen must be large enough [2].

The circuit also consists of bypass capacitors. One way to retain the desirable effect of R_E on bias stability and still achieve a large voltage gain is to connect a capacitor in parallel with R_E, shown as C_E in the Fig. 5. The capacitor should be large enough to have an impedance that is negligible in comparison to R_E at all frequencies of the ac signals. When this is the case, *the emitter is at ac ground* because the ac resistance in the emitter circuit is simply r_e. The capacitor effectively "short-out" R_E for ac signals, and it is called an emitter *bypass* capacitor, because it bypass ac signals around R_E to ground.

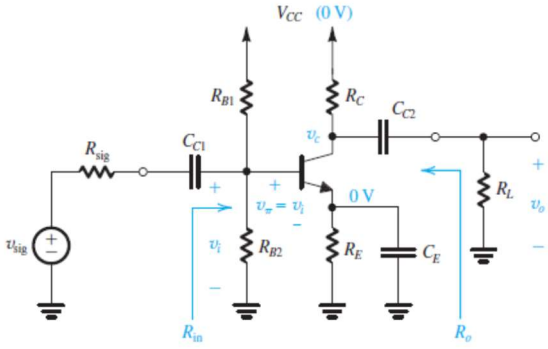

Figure 5. A Common-Emitter Configuration Amplifier with the Classical Biasing Arrangement

To determine the characteristic parameters of the CE amplifier above, we replace the BJT with its hybrid-π model, substitute V_{CC} with a short circuit to ground, and replace the coupling and bypass capacitors with short circuits. The small-signal equivalent circuit produced of the CE amplifier is shown in Fig. 6 below. The analysis is fairly easy and is given in those figure. Thus

$$R_{in} = R_{B1} \parallel R_{B2} \parallel r_\pi \tag{6}$$

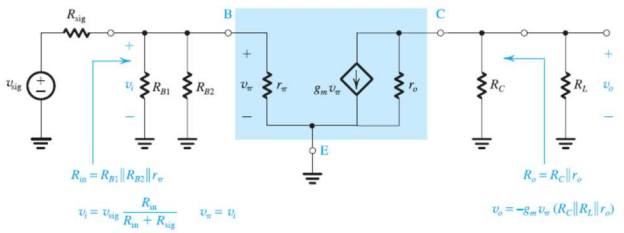

Figure 6. Equivalent Circuit and Analysis

which indicates that in order to keep R_{in} relatively high, the values of R_{B1} and R_{B2} should be selected large (typically in the range of tens or hundreds of kilohms). This requirement however is not inline with the need to keep R_{B1} and R_{B2} low so as to minimize the dependence of the dc current I_C on the transistor β (see section above).

The voltage gain G_v is calculated as follows. From Fig. 6, it can shown that at the input

$$v_i = v_{sig} \frac{R_{in}}{R_{in} + R_{sig}} \qquad \text{where } v_\pi = v_i$$

or $$v_{sig} = v_i \frac{R_{in} + R_{sig}}{R_{in}}$$

Therefore

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} \tag{7}$$

At the output

$$v_o = -g_m v_\pi (R_C \| R_L \| r_o) = -g_m v_i (R_C \| R_L \| r_o)$$

The voltage gain of this first stage, G_{v1}, is given by

$$G_{v1} = \frac{v_o}{v_i} = \frac{-g_m v_i (R_C \| R_L \| r_o)}{v_i} \tag{8}$$

$$= -g_m (R_C \| R_L \| r_o)$$

Note that we have taken r_o into account because it is convenient to do so. The effect of this parameter on discrete-circuit amplifier performance is, however, usually small.

FIRST STAGE DESIGN

At this first stage, a common-emitter amplifier will be designed as follows. Let $V_{CC} = +15\ V$, $\beta = 100$, and $V_{BE} \cong 0.7\ V$. This stage was designed to obtain $V_C = +8.2\ V$ (later, we will see the same case for the second stage design where V_C will also be made of magnitude $+8.2\ V$, because the voltage at the emitter lead of the common collector stage will be set to $8.2\ V - 0.7\ V = 7.5\ V$ in order to get maximum symmetrical swing of the final output signal). The collector current $I_E = 0.5\ mA$. The design is for a dc voltage at the base of 5 V (recall that we have to satisfy $V_{BB} \gg V_{BE}$) and a current through R_{B2} of $50\mu A$. This amplifier will operate a 10 $k\Omega$ source (i.e. $R_{sig} = 10\ k\Omega$).

We will calculate R_C and R_E as follows. First, we calculate R_C. From Fig. 5, it can be shown that

$$V_{CC} = V_C + I_C R_C \tag{9}$$

$$R_C = \frac{V_{CC} - V_C}{I_C} \rightarrow R_C = \frac{15 - 8.2}{0.5\ x\ 10^{-3}} = 13.6\ k\Omega$$

Next, to calculate R_E, we use the expression

$$V_B = V_{BE} + V_E \tag{10}$$

$$V_E = V_B - V_{BE} \rightarrow V_E = 5 - 0.7 = 4.3\ V$$

and

$$V_E = I_E R_E \rightarrow R_E = \frac{V_E}{I_E} = \frac{4.3}{0.5\ x\ 10^{-3}} = 8.6\ k\Omega$$

Next, R_{B1} and R_{B2} were calculated as follows. As a rule of thumb, we will design for V_{BB} about $\frac{1}{3}V_{CC}$, V_{CB} (or V_{CE}) about $\frac{1}{3}V_{CC}$, and $I_C R_C$ about $\frac{1}{3}V_{CC}$. We shall follow the rule and therefore allocate one-third of the supply voltage to the voltage drop across R_{B2} and another one-third to the voltage drop across R_C, leaving one-third for possible negative signal swing at the collector. Thus, $V_B = \frac{15\ V}{3} = +5\ V$ (as mentioned above) and the magnitude of V_E and R_E are determined as above.

The value of R_{B1} and R_{B2} are calculated as follows. From the discussion of equation (5), we therefore select a voltage-divider current of $0.1I_E = 0.1\ x\ 0.5\ mA = 0.05\ mA = 50\mu A$ (and indeed this design is for current through R_{B2} of $50\mu A$). The magnitude of R_{B2} is therefore $R_{B2} = \frac{5\ V}{50\ \mu A} = 100\ k\Omega$. Taking into account the non-zero base current, we have the base current $I_B = \frac{I_C}{\beta} = \frac{\alpha I_E}{100} = \frac{0.99\ x\ 0.5\ mA}{100} \cong \frac{0.5\ mA}{100} \cong 5\ \mu A$. Thus, a base current of magnitude $5\ \mu A$ will flow toward the base. Since the current through resistor R_{B2} to be of magnitude $50\ \mu A$, so the current through resistor R_{B1} become $50\ \mu A + 5\ \mu A = 55\ \mu A$. Then, since the design is for a dc voltage at the base of 5 V, so we have a voltage of $15\ V - 5\ V = 10\ V$ accross the resistor R_{B1}. The value of R_{B1} therefore can be calculated as $R_{B1} = \frac{v_{R_{B1}}}{i_{R_{B1}}} = \frac{10\ V}{55\ \mu A} = 181{,}818.181\ \Omega$. We pick a resistor of magnitude 182 kΩ for this R_{B1}. To recapitulate thus, for this first stage design we will have $R_C = 13.6$ kΩ, $R_E = 8.6$ kΩ, $R_{B1} = 182$ kΩ, and $R_{B2} = 100$ kΩ .

The circuit for this first stage was then simulated with NI Multisim as shown in Fig. 7 below. We perform a Multisim interactive simulation. It can be shown in the simulation that voltage at the base $V_B = 4.99V$ and the voltage at the collector (at the point before the collector coupling capacitor) is $V_{dc} = 8.14\ V$. However, at the point after the coupling capacitor, $V_{dc} = 1.08\ \mu V$ and $V_{p-p} = 609\ \mu V$. This shows that the coupling capacitor indeed blocking the dc component and leaving only the ac component $V_{p-p} = 604\ \mu V$. For the current, the emitter current $I_E = 510\ \mu A$, the collector current $I_C = 505\ \mu A$, and the current through $R_{B2} = 49.9\ \mu A$. These all are in excellent agreement with the requirement.

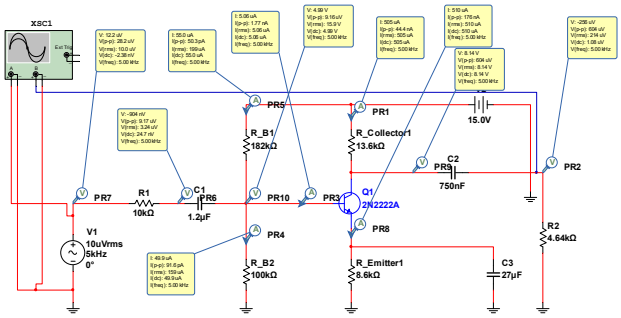

Figure 7. First Stage Circuit Interactive Simulated with NI Multisim

For a BJT, we have a parameter called g_m, which is the **transconductance** of the transistor, given by

$$g_m = \frac{I_C}{V_T} \tag{11}$$

and

$$r_\pi = \frac{\beta}{g_m} \tag{12}$$

where I_C is the the dc bias value and $V_T = thermal\ voltage = \frac{kT}{q} \cong 25$ mV at room temperature. At $I_C = 0.5\ mA$, we therefore obtain values $g_m = \frac{0.5\ mA}{0.025\ V} = 20\ mA/V$ and $r_\pi = \frac{100}{20\ mA/V} = 5\ k\Omega$. For calculating r_o, we use the following expression

$$r_o = \frac{V_A}{I_C} \tag{13}$$

For the calculation of r_o, let $V_A = 100\ V$. We therefore obtain the value of $r_o = \frac{100\ V}{0.5\ mA} = 200k\Omega$. We are now able to calculate the value of R_{in} by using equation (6). The result is $R_{in} = 182\ k\Omega \parallel 100\ k\Omega \parallel 5\ k\Omega = 4.64\ k\Omega$.

Now, the value of of the gain can be calculated by using equation (6) and equation (7) as follows. The gain will be calculated with $R_L = R_{in2} = R_{in1}$. Note that R_{in2} is input resistance of the second stage. In other word, the input resistance of the second stage, R_{in2}, will act as the load resistance of the first stage.

From equation (7), we obtain

$$\frac{v_i}{v_{sig}} = \frac{R_{in}}{R_{in} + R_{sig}} = \frac{4.64}{4.64 + 10} \cong 0.32$$

And then, from equation (8) we obtain

$$\begin{aligned} G_{v1} &= -\ g_m\ (R_C \| R_L \| r_o) \\ &= -\ 20\ (13.6 \| 4.64 \| 200) \\ &= -\ 68.02\ V/V \end{aligned}$$

When simulated by using interactive simulation, the following results were obtained. By using an ac signal of 28.2 μV (p-p) at 5kHz of frequency (i.e. $V_{sig(p-p)} = 28.2\ \mu V$), we obtain an input voltage of magnitude 9.17 μV (p-p), and an output voltage of

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magnitude -604 μV (p-p). Therefore, the overall voltage gain for this first stage is $\frac{v_{o(p-p)}}{v_{sig(p-p)}} = \frac{-604\ \mu V}{9.17\ \mu V} = -65.87\ \frac{V}{V}$.

Figure 8 below shows the NI Multisim Oscilloscope Instrument Simulation for the output signal, $v_{o(p-p)}$ (shown in blue, with 100 $\frac{\mu V}{Div}$ vertical scale) and the input signal (shown in red, with 10 $\frac{\mu V}{Div}$ vertical scale).

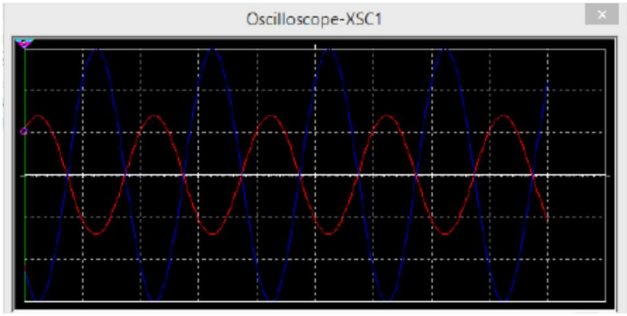

Figure 8. Output and Input Signals of the first stage Shown by NI Multisim Oscilloscope Instrument Simulation

Again, the simulation result is in quiet agreement with the above result calculated for the gain of $-68.02\ \frac{V}{V}$.

SECOND STAGE DESIGN

At this second stage, again a common-emitter configuration amplifier was designed. We will impose exactly the same requirement as in the first stage CE. Thus, emitter current $I_E = 0.5\ mA$ (which means that I_C, the current flowing through R_C is also to be $\cong 0.5\ mA$). Again, let we have $V_{CC} = +15\ V$, $\beta = 100$, and $V_{BE} \cong 0.7\ V$. And the design is again for a dc voltage at the base of 5 V. Finally, the load is 300 Ω. Thus, for this second stage design we will have $R_C = 13.6\ k\Omega$, $R_E = 8.6$ kΩ, $R_{B1} = 182$ kΩ, and $R_{B2} = 100$ kΩ.

Next, here we again have a parameter called g_m and r_π, whose magnitude are the same as those for the first stage (since magnitude the collector current, I_C, for this second stage is also 0.5 mA). Thus, $g_m = 20\ mA/V$ and $r_\pi = \frac{100}{20\ mA/V} = 5\ k\Omega$. For the calculation of r_o, we also obtain the value of $r_o = 200k\Omega$. This is because the value of I_C is the same

To calculate the gain of this second stage, we replace the entire amplifier circuit with its small-signal equivalent circuit as follows

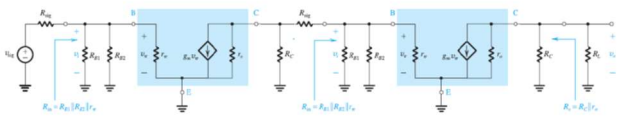

Figure 9. Small-Signal Equivalent Circuit of the First Stage and the Second Stage Amplifier

The input resistance of the second stage, R_{in2}, is

$$R_{in2} = R_{B1} \parallel R_{B2} \parallel r_\pi$$

Since the magnitude of R_{B1}, R_{B2}, and r_π is the same as those for the first stage, so $R_{in2} = R_{in}$.

Now, we can calculate the value of gain of this second stage. From Fig. 9 above, it can be shown that at the input side the input voltage

$$v_{b2} = v_\pi$$

and at the output side the output voltage

$$v_o = -g_m v_\pi (R_C \| R_L \| r_o)$$

Therefore, the value of $\frac{v_o}{v_{b2}} = G_{v2}$ is

$$G_{v2} = \frac{v_o}{v_{b2}} = -\frac{-g_m v_\pi (R_C \| R_L \| r_o)}{v_\pi} = -g_m (R_C \| R_L \| r_o)$$

By substituting the values of $g_m = 20\frac{mA}{V}$, $R_C = 13.6\ k\Omega$, $R_L = 300\ \Omega$, and $r_o = 200\ k\Omega$ we have

$$G_{v2} = \frac{v_o}{v_{b2}} = -20\ (13.6 \parallel 0.3 \parallel 200) = -5.87\ V/V$$

Now, we can calculate the entire amplifier' overall gain. That is,

$$\begin{aligned} G_{overall} &= \frac{v_o}{v_{sig}} = \frac{v_o}{v_{b2}}\ x\ \frac{v_{b2}}{v_{b1}}\ x\ \frac{v_i}{v_{sig}} \\ &= \frac{v_o}{v_{b2}}\ x\ \frac{v_{b2}}{v_{b1}}\ x\ \frac{v_{b1}}{v_{sig}} \\ &= -5.87\ x\ -68.02\ x\ 0.32 = 127.77\ V/V \end{aligned}$$

Note that at the first stage, $v_i = v_{b1}$

A resistor of magnitude 300 Ω was then placed to act as a load. The circuit with this second stage included was again simulated by using interactive simulation. The result of the simulation is shown in Fig. 10 below. It can be shown in that simulation, at the second stage, that voltage at the base V_B is $V_{dc} = 4.99\ V$ and the voltage at the collector (at the point before the collector coupling capacitor) is $V_{dc} = 8.15\ V$. After the collector coupling capacitor, it can be seen that we have $V_{p-p} = 3.41\ mV = 3410\ \mu V$ and V_{dc} in order of $-82.7\ nV$. This again shows that the coupling capacitor of this second stage indeed blocking the dc component and leaving only the ac component $V_{p-p} = 3.41\ mV$. For the current, the emitter current $I_E = 509\ \mu A$, the collector current $I_C = 504\ \mu A$, and the current through $R_{B2} = 49.9\ \mu A$.

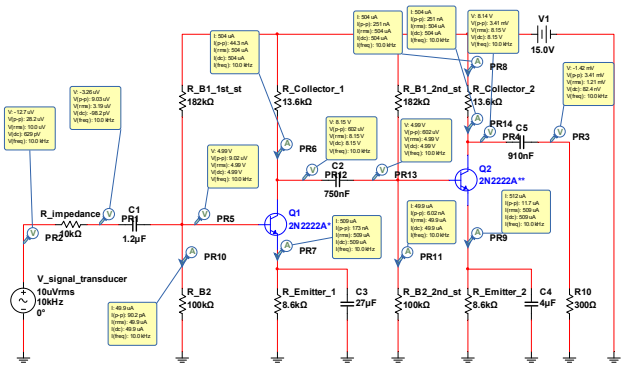

Figure 10. First Stage and Second Stage Circuit Interactive Simulated with NI Multisim

From the results of the simulation, the overall gain of the entire circuit can be calculated as follows

$$G_{overall} = \frac{v_o}{v_{si}} = \frac{v_{o(p-p)}}{v_{sig(p-p)}} = \frac{3410\ \mu V}{28.2\ \mu V} = 120.92\ V/V$$

It can be seen that in the simulation using NI Multisim, the overall gain $G_{overall} = 120.92\ V/V$, while from the calculation the overall gain $G_{overall} = 127.77\ V/V$. This simulation result is also in quiet agreement with the calculated result.

THIRD STAGE DESIGN

Up to the second stage design in the previous section, we notice that the overall gain of those two-stages amplifier is only $120.92\ V/V$. This is far from the expectation that the overall gain for the entire two-stages should be approximately $-68.02\frac{V}{V} \times -68.02\frac{V}{V} \times 0.32 = 1480.55\frac{V}{V}$ since the first stage common-emitter and the second stage common emitter are exactly the same.

As we have discovered, the input impedance (R_{in}) of the common-emitter (CE) amplifier is moderate-to-high (on the order of a few $k\Omega$, which is $4.64\ k\Omega$ here). The output impedance (R_{out}) is high (roughly the value of R_C, which is $13.6\ k\Omega$ here). This makes the Common-Emitter amplifier a poor choice for "driving" small loads (note that the load here is $300\ \Omega$). Thus, at this third stage, it was considered that the output impedance has to be low. This condition could be achieved by using a buffer.

A common-collector (CC) amplifier, however, typically has a **high input impedance** (typically in the hundred $k\Omega$ range) and a very **low output impedance** (on the order of $1\ \Omega$ or $10\ \Omega$). This makes the common-collector amplifier excellent for "driving" small loads. This common-collector amplifier has a voltage gain of about 1, or **unity gain**. The common-collector amplifier is considered a **voltage-buffer** since the voltage gain is unity. The voltage signal applied at the input will be duplicated at the output; for this reason, the common-collector amplifier is typically called an **emitter-follow amplifier**. The common-collector amplifier can be thought of as a **current amplifier** [16].

When the common-emitter amplifier on the second stage above is cascaded to a common-collector amplifier, the CC amplifier can be thought of as an "**impedance transformer**." It can take the high output impedance of the CE amplifier and "transform" it to a low output impedance capable of driving small loads.

Figure 11(a) shows an emitter follower (with the bias circuit omitted) with the equivalent circuit shown in Fig. 11(b).

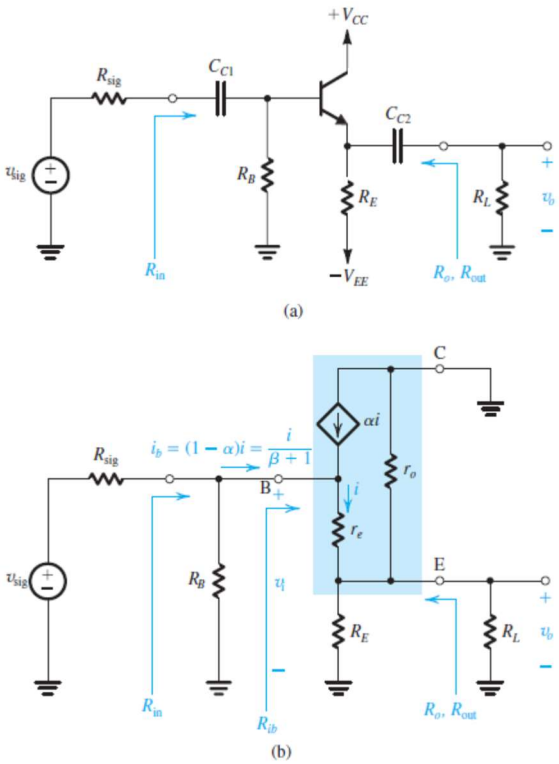

Figure 11. (**a**) An emitter follower circuit. (**b**) Small-signal equivalent circuit of the emitter follower with the transistor replaced by its T model. Note that r_o is included because it is easy to do so. Normally, its effect on performance is small.

The input resistance R_{in} is found from

$$R_{in} = \frac{v_i}{i_{in}} = \frac{v_i}{i_b} \tag{14}$$

Then, by writing Kirchhoff's voltage law from base B to ground in Fig 11(b) and by substituting $i_b(\beta + 1)$ for i_e, we obtain

$$\begin{aligned} v_i &= i_e r_e + i_e R_E \\ &= i_b(\beta + 1) r_e + i_b(\beta + 1) R_E \\ &= i_b(\beta + 1)(r_e + R_E) \end{aligned} \tag{15}$$

Substituting (15) into (14), we find

$$R_{in} = \frac{i_b(\beta + 1)(r_e + R_E)}{i_b} = (\beta + 1)(r_e + R_E) \tag{16}$$

Again invoking the approximation $\beta + 1 \approx \beta$, we have

$$R_{in} = (\beta + 1)(r_e + R_E) \approx \beta(r_e + R_E) \tag{17}$$

In many practical circuits, $R_E \gg r_e$, so R_{in} can usually be computed simply as

$$R_{in} \approx \beta R_E \tag{18}$$

It is apparent from Fig. 11(b) that

$$R_{in}(stage) = R_B \| R_{in} \approx R_B \| \beta R_E \tag{19}$$

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Equations (17) and (18) reveal the single most important feature of CC amplifier in practical applications; its input resistance, R_{in}, can be made very large in comparison to the other configurations. For example, using the typical values $R_E = 1\ k\Omega$ and $\beta = 100$, we have $R_{in} \approx 100\ k\Omega$, which is a **high input impedance.**

The output voltage in the CC configuration is the collector-emitter voltage. Since the collector is grounded, the ac output voltage is the same as the emitter-to-ground voltage. We can therefore derive the voltage gain of the CC transistor as follows

$$A_v = \frac{v_o}{v_{in}} = \frac{i_e R_E}{v_{in}} \tag{20}$$

Substituting from equation (15) for v_{in}, in equation (20), we obtain

$$A_v = \frac{i_e R_E}{v_{in}} = \frac{i_e R_E}{i_b(\beta + 1)(r_e + R_E)} \tag{21}$$

$$= \frac{i_b(\beta + 1)R_E}{i_b(\beta + 1)(r_e + R_E)} = \frac{R_E}{r_e + R_E}$$

Since $r_e + R_E > R_E$, equation (20) shows that the CC transistor always has a voltage gain less than 1. It is usually the case that $R_E \gg r_e$, so the following approximation is often used:

$$A_v = \frac{R_E}{r_e + R_E} \approx \frac{R_E}{R_E} = 1 \tag{22}$$

Equation (22) states that $\frac{V_o}{V_{in}}$ is (approximately) 1, from which it follows that $v_o \approx v_{in}$. Thus, as stated above, the voltage signal applied at the input will be duplicated at the output.

It is not difficult to visualize why the ac output voltage is approximately the same as the ac input voltage in a CC configuration: the input and output are "separated" only by the small ac resistance of the forward-biased base-emitter junction, r_e (see Fig. 11(b)). In other words, the input (base-to-ground) voltage is the same, except for the small drop across the junction, as the output (emitter-to-ground) voltage. Note that there is no phase inversion between input and output. As the base-to-ground voltage increase, so does the emitter-to-ground voltage. Since the output voltage is essentially the same as the input voltage, in magnitude and phase, the emitter is said to *follow* the base. In that context, a transistor in the CC configuration is often called an *emitter follower* (more often, in fact, than it is called a common-collector circuit).

The next step now is to connect the output of the second stage CE configuration to the input of this third stage *emitter follower* configuration.

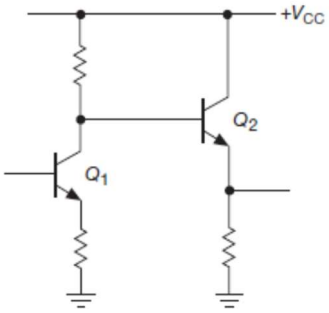

Figure 12. Biasing an Emitter Follower from a Previous Stage

When an *emitter follower* is driven from a preceding stage in a circuit, it is usually OK to connect its base directly to the previous stage's output, as shown in Fig. 12 above [17].

Because the signal on $Q_1's$ collector is always within the range of the power supplies, $Q_2's$ base will be between V_{CC} and ground, and therefore Q_2 is in the active region (neither cut off nor saturated), with its base–emitter diode in conduction and its collector at least a few tenths of a volt more positive than its emitter. Sometimes, though, the input to an emitter follower may not be so conveniently situated with respect to the supply voltages. A typical example is a capacitively coupled (or ac-coupled) signal from some external source (e.g., an audio signal input to a stereo amplifier) like the one in this multistage amplifier design here. In that case the signal's average voltage is zero, and direct coupling to an emitter follower will give an output like that in Fig. 13.

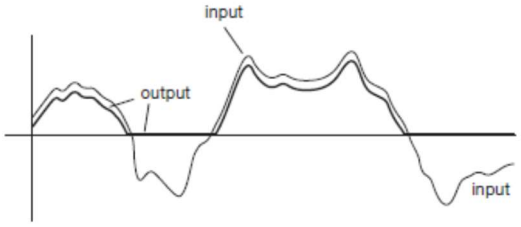

Figure 13. A Transistor Amplifier Powered from a Single Positive Supply Cannot Generate Negative Voltage Swings at the Transistor Output Terminal.

It is necessary to *bias* the emitter follower so that collector current flows during the entire signal swing. In this case a voltage divider is the simplest way (Fig. 14).

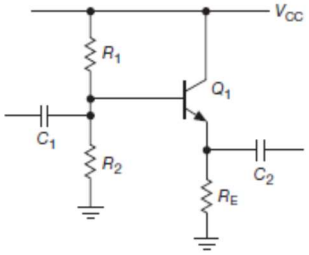

Figure 14. An AC-coupled Emitter Follower. Note Base Bias Voltage Divider.

Resistors R_1 and R_2 in Fig. 14 are chosen to put the base halfway between ground and V_{CC} when there is no input signal, i.e., R_1 and R_2 are approximately equal. The process of selecting the

operating voltages in a circuit, in the absence of applied signals, is known as setting the *quiescent point*. In this case, as in most cases, the quiescent point is chosen to allow maximum symmetrical signal swing of the output waveform without *clipping* (flattening of the top or bottom of the waveform). What values should R_1 and R_2 have? We make the impedance of the dc bias source (the impedance looking into the voltage divider) small compared with the load it drives (the dc impedance looking into the base of the follower). In this case,

$$R_1 \| R_2 \ll \beta R_E.$$

This is approximately equivalent to saying that the current flowing in the voltage divider should be large compared with the current drawn by the base.

In this design here, V_{CC} is $+15\ V$, and quiescent current is to be $1\ mA$.

Step 1. *Choose* V_E. For the largest possible symmetrical swing without clipping, $V_E = 0.5 \times V_{CC}$, or $+7.5\ V$ volts.

Step 2. *Choose* R_E. For a quiescent current of $1\ mA$ ($I_E = 1\ mA = 1000\ \mu A$) for example, $R_E = \frac{7.5\ V}{1\ mA} = 7.5\ k\Omega$.

Step 3. *Choose* R_1 *and* R_2. Base voltage V_B is $V_e + 0.7V$, or $7.5V + 0.7V = 8.2V$. This determines the ratio of R_1 to R_2 as $1 : 1.21$. The loading criterion requires that the load resistance of the second stage common-emitter should be $4.64\ k\Omega$. Note that the input resistance to the third stage emitter follower will act as the load resistance of the second stage common-emitter. By using the $300\ \Omega$ load, the ac load on the third stage is $r_L = 7.5\ k\Omega \parallel 300\ \Omega \approx 300\ \Omega$, so that the input resistance to the third stage emitter follower is

$$r_{in}\ (stage\ 3) = R_1 \| R_2 \| \beta (r_e + r_L) \qquad (23)$$

By trial error using $R_1 = 13\ k\Omega$ and $R_2 = 16\ k\Omega$, the following result for $r_{in}\ (stage\ 3)$ was obtained:

$$r_{in}\ (stage\ 3) = 13\ k\Omega \| 16\ k\Omega \| 100[(25\ \Omega) + (300\ \Omega)]$$
$$= 7.172\ k\Omega \| 32.5\ k\Omega = 5.875\ k\Omega$$

Note that for r_e, the value $r_e = \frac{0.025}{I_E}\ \Omega = \frac{0.025}{1\ mA} = 25\ \Omega$ was used The overall amplifier circuit of the first stage CE, the second stage CE, and the third stage CC was shown in Fig. 15 below. The circuit was then interactive simulated and the following results were obtained as shown in the figure: at the second stage common-emitter, the voltage at the base V_B is $V_{dc} = 4.99\ V$ and the voltage at the collector (at the point before the collector coupling capacitor) is $V_{dc} = 8.15\ V$. At the point before and after the collector coupling capacitor, it can be seen that this time we have $V_{(p-p)} = 46.4\ mV = 46400\ \mu V$ (not $V_{(p-p)} = 3.41\ mV$ anymore). At the base of the third stage, the dc voltage $V_{dc} = 8.21\ V$. This again shows that the coupling capacitor blocking the dc component from the second stage and leaving only the ac component $V_{(p-p)} = 46.4\ mV$. For the current, the emitter current $I_E = 509\ \mu A$, the collector current $I_C = 504\ \mu A$, and $I_{R_{B2}} = 49.9\ \mu A$ ($I_{R_{B2}}$ is the current through R_{B2})

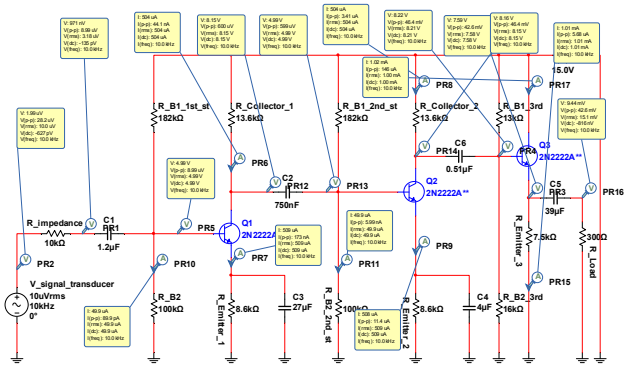

Figure 15. First Stage, Second Stage, and Third Stage Circuit (i.e. Overall Circuit) Interactive Simulated with NI Multisim

And finally, at the common-colector amplifier the following results were obtained: at the base lead, the dc voltage $V_{dc} = 8.21\ V$, the emitter current $I_E = 1.01\ mA$. At the emitter lead before the coupling capacitor, the dc voltage $V_{dc} = 7.58\ V$, and the ac voltage $V_{(p-p)} = 42.6\ mV = 42600\ \mu V$. At the point after the coupling capacitor, the dc voltage $V_{dc} = 3.15\ \mu V$ (again proving that the dc signal was blocked) and leaving only the ac component $V_{(p-p)} = 42.6\ mV = 42600\ \mu V$ accross the load.

Thus, From the results of the simulation, the overall gain of the entire circuit (i.e. the first stage common-emitter, the second stage common emitter, and the third stage emitter follower) can be calculated as follows

$$G_{overall} = \frac{v_o}{v_{sig}} = \frac{v_{o(p-p)}}{v_{sig(p-p)}} = \frac{42600\ \mu V}{28.2\ \mu V} = 1510.64\ \frac{V}{V}$$

This simulation result is again in quiet agreement with the result calculated. Recall that the calculated result for the overall gain was $-68.02\ \frac{V}{V} \times -68.02 \frac{V}{V} \times 0.32 = 1480.55\ \frac{V}{V}$.

Note that this is obviously a very significant improvement over the situation without using the emitter follower amplifier.

FREQUENCY RESPONSE

The *frequency response* of an electronic device or system is the variation it causes, if any, in the level of its output signal when the frequency of the signal is changed. In other words, it is the manner in which the device *responds* to changes in signal frequency.

The gain of an amplifier is a function of frequency. The frequency response of an amplifier is usually presented in the form of graph that shows output amplitude (or, more often, voltage gain) plotted versus frequency. Figure 16 shows a typical plot of the voltage gain of an ac amplifier versus frequency. Notice that the gain is 0 at dc (zero frequency), then rises as frequency increases, levels off for further increases in frequency, and then begins to drop again at high frequencies. The frequency range over which the gain is more or less constant ("flat") is called midband range

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Our study of transistor amplifiers has assumed that their gain is always constant for all of the input signal frequency. This would mean that their bandwidth is infinite, which of course is not right. To illustrate what is actually occuring, Fig. 16 below shows a sketch of the magnitude of the gain versus the frequency of the input signal of a discrete-circuit BJT amplifier. It clearly shows that there is indeed a wide frequency range over which the gain remains almost constant. This is the useful frequency range of operation for the particular amplifier.

As mentioned above, Fig. 16 below indicates that at lower frequencies, the magnitude of the amplifier gain begins to fall off. This occurs because the coupling and bypass capacitors no longer have low impedances. Recall that we assumed that their impedances were small enough to act as short circuits. As the frequency of the input signal is lowered, the capacitance reactance with magnitude $\frac{1}{j\omega C} = \frac{1}{2\pi f C}$ of each of these capacitors becomes significant. This results in a decrease in the overall voltage gain of the amplifier.

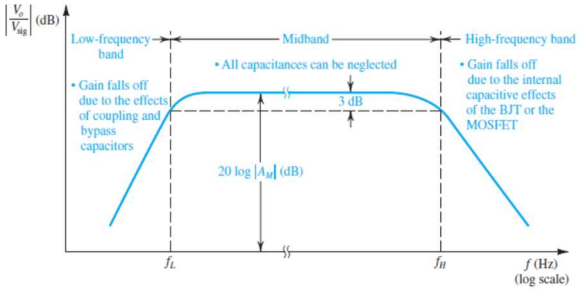

Figure 16. Sketch of the Magnitude of the Gain of a Discrete-Circuit BJT Amplifier Versus Frequency [15].

The decline in the overall gain due to low frequencies signal is also occured in the design of our voltage amplifier here. This section will now discuss about the low-frequency response of our multistages common-emmiter, common-collector amplifier. Here, we will investigate the effect of the coupling and bypass capacitors on our discrete-circuit common-emitter (CE) and common-collector (CC) amplifiers' gain.

We wish to obtain an estimate of the frequency f_L at which the gain of this amplifier drops by 3 dB below its value at midband (i.e. the gain becomes 0.707 x the gain value at midband. The multiplier 0.707 was chosen because at this level the output power is half the midband power output [18]). The appropriate values for C_{C1}, C_{C2}, and C_E for our common-emitter amplifier and common-collector amplifier then need to be selected in order to satisfied with the requirement for f_L.

To analyze the low-frequency gain of the first stage CE amplifier, we make use of the the equivalent circuit shown in Fig. 17 below. This equivalent circuit is obtained by short-circuiting V_{CC} and replacing the BJT with its *T*-model, while neglecting r_o.

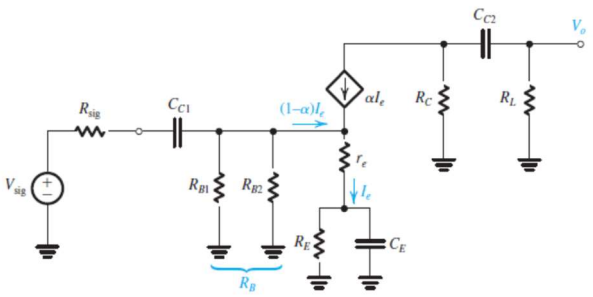

Figure 17. T Model, Equivalent Circuit, of the Discrete-Circuit Common-Emitter Amplifier

Recall that our first stage amplifier has $R_C = 13.6$ kΩ, $R_E = 8.6$ kΩ, $R_{B1} = 182$ kΩ, and $R_{B2} = 100$ kΩ , $R_L = 4.64\ k\Omega$, $R_{sig} = 10\ k\Omega$, $\beta = 100$, $g_m = 20\ mA/V$, and $r_\pi = 5\ k\Omega$. Suppose that it is required for our voltage amplifier circuit to have $f_L = 100\ Hz$.

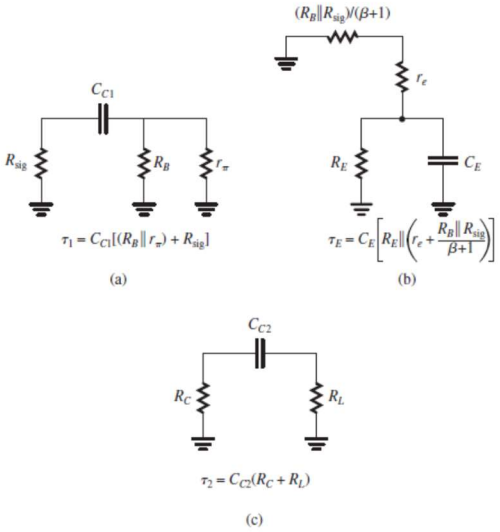

Figure 18. Circuits for determining the short-circuit time constants for the amplifier

Figure 18 above is circuits for determining the short-circuit time constants for the amplifier in Fig. 17. First, we will determine the resistances seen by the three capacitors C_{C1}, C_{C2}, and C_E as follows:

Refer to Fig. 18a, Capacitor C_{C1} sees a resistance R_{C1} as

$$R_{C1} = (R_B \| r_\pi) + R_{sig} \tag{23}$$

where

$$R_B = (R_{B1} \| R_{B2}) = (182\ k\Omega \| 100\ k\Omega) = 64.54\ k\Omega$$

$$R_{C1} = (64.54\ k\Omega \| 5\ k\Omega) + 10\ k\Omega = 14.64\ k\Omega$$

Refer to Fig. 18b, the total resistance R_{CE} seen by C_E is

$$R_{CE} = R_E \left\| \left[r_e + \frac{R_B \| R_{sig}}{\beta + 1} \right] \right. \tag{24}$$

where

$$r_e = \frac{V_T}{I_E} = \frac{25\ mV}{0.5\ mA} = 50\ \Omega$$

$$R_{CE} = 8.6\ k\Omega \left\| \left[50\ \Omega + \frac{64.54\ k\Omega \| 10\ k\Omega}{100+1} \right] \right.$$

$$R_{CE} = 8.6\ k\Omega \parallel 135.73\ \Omega$$

$$R_{CE} = 133.62\ \Omega = 0.13362\ k\Omega$$

Finally by refering to Fig. 18c, the resistance R_{C2} seen by C_{C2} is

$$R_{C2} = R_C + R_L = 13.6\ k\Omega + 4.64\ k\Omega = 18.24\ k\Omega \quad (25)$$

We calculate the 3-dB frequency f_L by using an expression

$$f_L \cong \sum_{i=1}^{n} \frac{1}{C_i R_i} \quad (26)$$

where *n* is the total number of capacitors.

Now, selecting C_E so that it contributes 80% of the value of ω_L gives

$$\frac{1}{C_E\ x\ 133.62} = 0.8\ x\ 2\pi\ x\ 100$$

$$C_E = 14.89\ \mu F$$

Next, if C_{C1} is to contribute 10% of f_L,

$$\frac{1}{C_{C1}\ x\ 14.64\ x\ 10^3} = 0.1\ x\ 2\pi\ x\ 100$$

$$C_{C1} = 1.09\ \mu F$$

Similarly, if C_{C2} is to contribute 10% of f_L, its value should be selected as follows:

$$\frac{1}{C_{C2}\ x\ 18.24\ x\ 10^3} = 0.1\ x\ 2\pi\ x\ 100$$

$$C_{C2} = 0.873\ \mu F$$

To recapitulate, for this first stage we have $C_{C1} = 1.09\ \mu F$, $C_{C2} = 0.873\ \mu F$, and $C_E = 14.89\ \mu F$ for the coupling and bypass capacitors. Choosing standard capacitors with the next highest values, we select $C_{C1} = 1.1\ \mu F$, $C_{C2} = 0.91\ \mu F$, and $C_E = 15\ \mu F$

For the second stage, again we use the equivalent circuit, *T*-model in Fig. 17 to analyze the low-frequency gain. This time, we need to determine C_{C2} and C_E. Like before, we first determine the resistances seen by the two capacitors C_{C2}, and C_E as follows:

$$R_{CE} = R_E \left\| \left[r_e + \frac{R_B}{\beta+1} \right] \right.$$

$$R_{CE} = 8.6\ k\Omega \left\| \left[50\ \Omega + \frac{64.54\ k\Omega}{100+1} \right] \right.$$

$$R_{CE} = 8.6\ k\Omega \| \left[689.01\ \Omega \right]$$

$$R_{CE} = 637.90\ \Omega$$

Note that there is no R_{sig} term anymore inside the expression for calculating R_{CE} for this second stage.

Then for R_{C2} ,

$$R_{C2} = R_C + R_L = 13.6\ k\Omega + 5.875\ k\Omega = 19.475\ k\Omega$$

Again, for this second stage, we select *CE* so that it contributes 80% of the value of ω_L, which gives us

$$\frac{1}{C_E\ x\ 637.90} = 0.8\ x\ 2\pi\ x\ 100$$

$$C_E = 3.12\ \mu F$$

In order to determine the value of C_{C2}, we must note that this C_{C2} was connected to the third stage, a common collector (CC) amplifier. Thus, this C_{C2} belongs to the CC amplifier. This CC amplifier also has another capacitor connected between the load and its emitter. The capacitor values necessary to achieve specified break frequencies in a common collector amplifier can be calculated as follows (now refer to Fig. 14)

$$C_2 = \frac{1}{2\pi(R_e + R_L) f_L (C_2)} \quad (27)$$

where

$$R_e = R_E \| \left(\frac{r_S \| R_1 \| R_2}{\beta} + r_e \right) \quad (28)$$

$$C_1 = \frac{1}{2\pi [r_{in}(stage) + r_S] f_L (C_1)} \quad (29)$$

where

$$r_{in}(stage) = R_1 \| R_2 \| \beta (r_e + R_E \| R_L)$$

The value of C_2 will be selected first. To obtain a value for R_e, we must first find the value of r_e:

$$r_e \approx \frac{0.025}{I_E} = \frac{0.025}{1\ mA} = 25\ \Omega$$

Then, from equation (28),

$$R_e = 7.5\ k\Omega \| \left(\frac{10\ k\Omega \| 13\ k\Omega \| 16\ k\Omega}{100} + 25\ \Omega \right)$$

$$R_e = 7.5\ k\Omega \parallel 66.77\ \Omega \approx 66.18\ \Omega$$

To find C_2 and C_1, we let $f_L(C_2) = f_L(C_1) = 100\ Hz/10 = 10\ Hz$, and then use equation (27) to calculate

$$C_2 = \frac{1}{2\pi(66.18\ \Omega + 300\ \Omega) 10\ Hz} = 43.46\ \mu F$$

Note that the load resistor is $300\ \Omega$.

For C_1, we first calculate $r_{in}(stage)$

$$r_{in}(stage) = 13\ k\Omega \| 16\ k\Omega \| 100(25\ \Omega + 7.5\ k\Omega \| 300\ \Omega)$$
$$= 13\ k\Omega \| 16\ k\Omega \| 31.346\ k\Omega = 5.84\ k\Omega$$

Next, by using $r_S = 10\ k\Omega$, and then use equation (29) to calculate C_1, we obtain:

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$$C_1 = \frac{1}{2\pi[5.84\ k\Omega + 10\ k\Omega]10\ Hz} = 1.0\ \mu F$$

To recapitulate, for the second stage (CE) and the third stage (CC) we have the coupling capacitor between second stage common-emitter and third stage common-collector $C_1 = 1.0\ \mu F$, bypass capacitor $C_E = 3.12\ \mu F$, and $C_2 = 43.46\ \mu F$. Choosing standard capacitors with the next highest values, we select $C_1 = 1.1\ \mu F$, $C_2 = 47\ \mu F$, and $C_E = 3.3\ \mu F$.

The overall amplifier circuit with all the capacitors values as calculated above was again simulated with the interactive simulation of NI Multisim. This time, we also measure the frequency response in addition to the voltage gain measurement. The circuit of Fig 19. below shows the result of the interactive simulation, with an input signal magnitude of $10\ \mu V\ (rms)$ and frequency of $10\ kHz$.

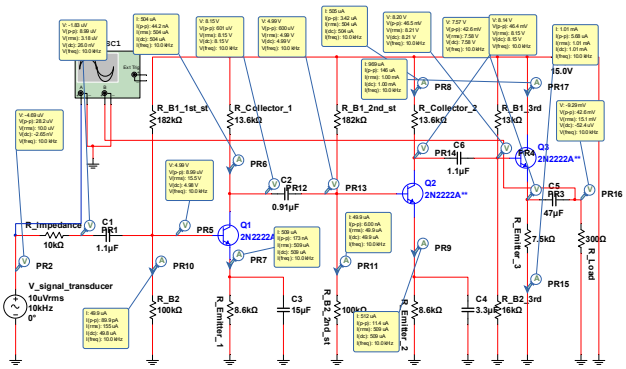

Figure 19. Interactive Simulation of the Overall Amplifier with the Coupling and Bypass Capacitors

It can be shown from the figure that all the various dc operating points of the circuit remain the same. The overall voltage gain of the circuit also does not change. (i.e. $G_{overall} = \frac{42600\ \mu V}{28.2\ \mu V} = 1510.64\ V/V$). Then, Fig. 20 below shows the NI Multisim Oscilloscope Instrument Simulation for the output signal (shown in red, with a $10\ \frac{mV}{Div}$ vertical scale) and the input signal (shown in blue, with a $100\ \frac{\mu V}{Div}$ vertical scale).

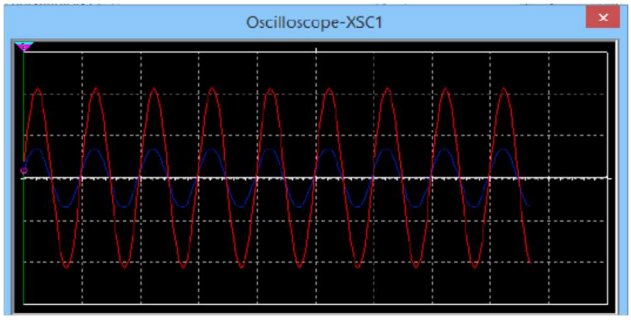

Figure 20. Output and Input Signals Shown in NI Multisim Oscilloscope Instrument Simulation

Next, the frequeny response of the circuit was analysed by performing an AC sweep analysis and simulation. The result of which is shown by Fig. 21 below. The response indicates that at a frequency of about 200 Hz, the magnitude of the amplifier gain begins to fall off. This is in agreement with the calculation above.

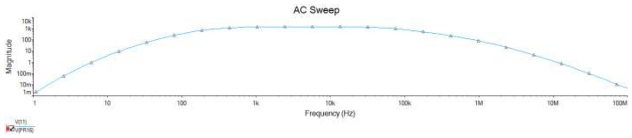

Figure 21. AC Sweep Analysis and Simulation of the Overall Amplifier Circuit

The frequency response of Fig. 21 above also indicates that the gain of the amplifier falls off at the high-frequency end. This is due to internal capacitive effects in the BJT.

CONCLUSIONS AND FUTURE WORKS

The three-stage voltage amplifier has been designed, simulate, and analysed in this research. Some important conclusions and future works can be drawn as follows.

Conclusions

Several conclusions that can be drawn is as follows.

1. A multistages ac voltage amplifier has been succesfully designed in this research which consists of a discrete-circuit amplifier called the common-emitter (CE) for providing the first gain, another CE amplifier which increase the overall gain required from the entire circuit, and a third output stage common-collector (CC) configuration which was used as a voltage buffer for connecting a high-resistance source to a low-resistance load.

2. The entire amplifier circuit has been succesfully simulated. By using an interactive simulation, it can be shown that the overall circuit functions properly in terms of the dc operating points and the voltage gain, in accordance with the calculated results. The simulation generate overall gain of magnitude about $1510\ \frac{V}{V}$ which is in accordance with the design purpose to provide small signal gain of about $1500\ \frac{V}{V}$.
3. The frequency response of the entire amplifier circuit has been successfully analysed by using the ac sweep analysis. The frequency f_L at which the gain of this amplifier drops by 3 dB below its value at midband (i.e. the gain becomes $0.707\ x$ the gain value at midband) is around 200 Hz.

Future Works

Some future works that could be performed further on this research are as follows :

1. The upper frequency (i.e. the higher frequency) at which the gain of this amplifier drops by 3 dB below its value at midband could also be analysed.
2. Other methods of coupling, such as direct coupling, can also be investigated for comparison. There are many applications in which it is important that the amplifier maintain its gain at low frequencies down to dc. Furthermore, monolithic integrated-circuit (IC) technology does not allow the

fabrication of large coupling capacitors. Thus IC amplifiers are usually designed as **directly coupled** or **dc amplifiers** (as opposed to **capacitively coupled**, or **ac amplifiers**).

3. There are still some other useful simulations that can be performed on this multistages CE amplifier circuit. This includes for example the noise analysis, distortion analysis and parameter sweep analysis.

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