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Minimizing THD Using a Multilevel Inverter Integrated with MPPT

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A B S T R A C T

This paper presents a novel Modified Multilevel Inverter (MMLI) topology to reduce Total Harmonic Distortion (THD) in photovoltaic (PV) systems. Unlike conventional Cascaded H-Bridge Inverters, the proposed MMLI achieves higher output voltage levels using fewer switching components by optimizing the arrangement of voltage sources and switches. A Boost converter integrated with Maximum Power Point Tracking (MPPT) further enhances power conversion efficiency and system stability. This specific configuration has not been previously explored, offering a more effective solution for THD mitigation. Simulations conducted in MATLAB/Simulink demonstrate the inverter's performance, with the 5-level MMLI achieving a THD of 28.99% and the 9-level configuration reducing it to 18.15%. These results confirm the superiority of the proposed topology in improving power quality and reducing system complexity. Moreover, the design eliminates the need for external filters, making it a cost-effective and practical option for grid-connected PV applications.

INTRODUCTION

The increasing global demand for clean and sustainable energy has accelerated the adoption of photovoltaic (PV) systems due to their environmentally friendly characteristics and declining installation costs. In 2023, global PV installations surpassed 1,000 GW, with annual capacity additions exceeding 100 GW, positioning solar energy as a strong alternative to fossil fuels [1]–[3]. Despite this growth, the efficiency of PV systems is still constrained by their power conversion stages, especially in the DC-to-AC process handled by inverters [4], [5].

Inverters play a vital role in PV systems by converting variable DC power from solar modules into stable AC power compatible with grid requirements. However, conventional inverter topologies, such as the Cascaded H-Bridge (CHB) inverter, tend to produce high Total Harmonic Distortion (THD), which degrades power quality, increases energy losses, and affects compliance with grid standards [6], [7]. Furthermore, the performance of inverters significantly influences overall system efficiency, particularly under variable irradiance and temperature conditions [8].

Multilevel inverters (MLIs) have gained attention for their ability to synthesize near-sinusoidal waveforms using multiple voltage levels, thus reducing THD. However, traditional MLI configurations often require a large number of switches and DC sources to achieve higher levels, resulting in increased complexity, cost, and switching losses [4], [9]. This complexity poses challenges for practical implementation, especially in compact or cost-sensitive PV applications.

To improve energy harvesting, Maximum Power Point Tracking (MPPT) techniques are commonly integrated into PV systems. Methods such as Perturb and Observe (P&O), Incremental Conductance (INC), and fuzzy logic have been widely used for MPPT control [10]–[14]. These algorithms aim to track the optimal operating point of PV modules under changing environmental conditions. However, many of these techniques suffer from slow response, oscillations around the MPP, or increased computational requirements [15]–[17].

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Some researchers have explored the integration of MPPT controllers with multilevel inverters to optimize both energy extraction and power quality. For example, hybrid systems using Adaptive Neuro-Fuzzy Inference Systems (ANFIS) and metaheuristic algorithms have shown promising results in reducing THD and improving MPPT efficiency [18]–[20]. Nevertheless, these systems often rely on complex control structures or require external filters to meet harmonic standards, which adds cost and design overhead [21], [22].

Based on these issues, this study addresses two primary problems: (1) the high THD generated by conventional inverter topologies in PV systems, and (2) the large number of switches and components required to achieve high voltage levels in traditional MLIs. To overcome these challenges, this paper proposes a Modified Multilevel Inverter (MMLI) topology with a simplified structure that minimizes switching devices while increasing the number of output levels. In addition, the proposed system integrates a Boost converter with an MPPT algorithm to enhance energy conversion efficiency and system stability without relying on external filtering.

The objective of this study is to design, simulate, and evaluate a novel MMLI-based inverter topology that: (i) reduces THD in PV systems; (ii) minimizes the number of components; and (iii) improves energy efficiency through MPPT-based DC-DC conversion. The performance of the proposed system is validated through simulations in MATLAB/Simulink, with comparative analysis against conventional CHB topologies under various switching configurations.

METHODS

Initially, it was about making a new topology to work on the cascaded multi-level inverter. The cascaded inverters come in different types; one of the types of cascaded inverters uses the flying capacitor type, while the other variant uses the clamped diode type. Since the meaning of cascading is the joining of two basic units of a similar kind of inverters together, the theory about cascading is that when the generated levels approach infinity, then the THD approaches zero, and by cascading more units together, this can be achieved. Well, the issue that arose by doing this thing is that the switches' numbers increase and it complicates the working of the switches. So, topology must be made so that it is less bulky, and the operations regarding lowering THD become easy. Other than that, a comparison must also be made with the existing topology. So, the comparison has been made with the H-Bridge cascaded topology under the same environment as the proposed topology to make sure that accurate results are achieved.

Modified Multilevel Inverter (MMLI) topology

The topology that was proposed was referred to as the Modified Inverter topology. The Modified Inverter is the H-bridge inverter circuit, where the location of the load can be replaced, and a short-circuit can be introduced. Switches are employed in this cell to have a boost effect, like in any boost converter. In the circuit, voltages tend to operate as the source elements to provide a constant output, but these can be replaced with any other DC source that can provide a continuous supply (i.e., PV arrays). The H-Bridge inverter includes different sources for each basic unit cell, while the Modified Inverter includes different sources for each basic unit cell as well. The basic unit of the proposed Modified Multilevel Inverter (MMLI) comprises four power switches and two isolated DC voltage sources, as illustrated in Figure 1. This configuration allows the generation of multiple voltage levels by appropriately controlling the switching states of the transistors. By arranging various such units in a cascaded structure, higher output levels can be achieved with fewer components than conventional topologies. This approach reduces the overall switch count and system complexity while maintaining high-quality output waveforms, improving power conversion efficiency, and lowering Total Harmonic Distortion (THD).

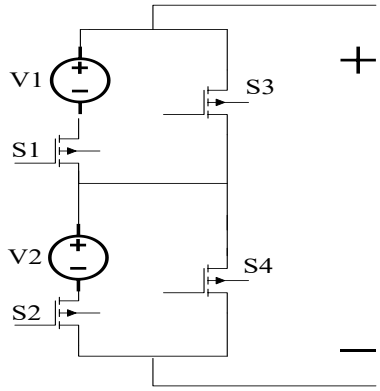

Figure 1: Figure 1. Basic unit of the proposed Modified Multilevel Inverter (MMLI) topology

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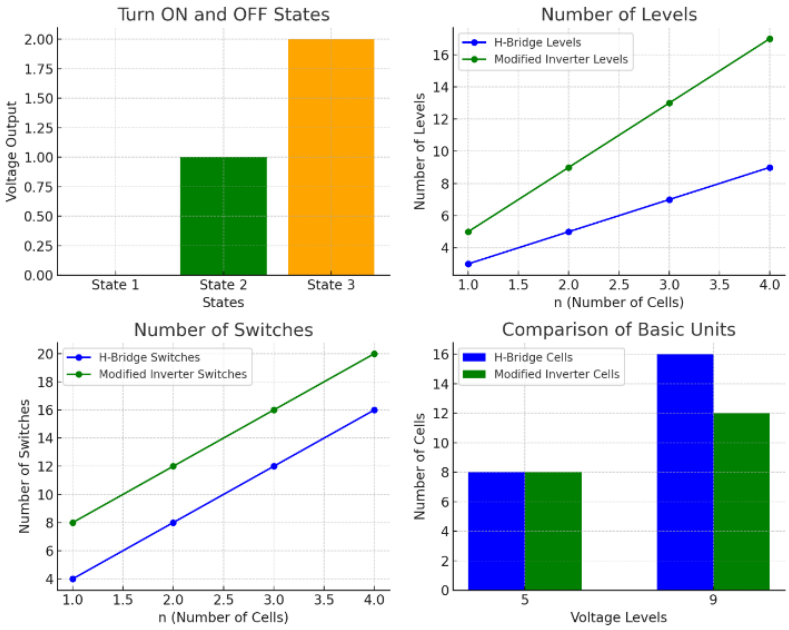

Figure 2. Comparison of Basic Units

Figure 2 provides a detailed comparative analysis of key features between H-Bridge and Modified Multilevel Inverter (MMLI) topologies. The first component of the figure, the bar chart depicting Turn ON and OFF States, illustrates the voltage outputs produced by various switching states. This demonstration is crucial as it highlights the operational states of the inverter that generate varying voltage levels, which are essential for optimizing power conversion efficiency.

Subsequently, the line graph comparing the Number of Levels illustrates how both the H-Bridge and Modified Inverters achieve different voltage levels as the number of cells (n) increases. The data indicate that the Modified Inverter can generate more voltage levels with the same number of cells, underscoring its enhanced performance in reaching higher voltage outputs.

Furthermore, the graph detailing the Number of Switches reinforces this advantage by contrasting the number of switches required by each inverter topology. It is evident that, as the number of cells increases, the Modified Inverter consistently requires fewer switches compared to the H-Bridge, thereby demonstrating superior design efficiency and reduced complexity.

Finally, the bar chart that compares Basic Units focuses on the number of basic cells necessary to achieve specific voltage levels—5 and 9 levels. This analysis reveals that while both inverters require the same number of cells to produce a 5-level output, the H-Bridge necessitates significantly more cells to achieve a 9-level output than the Modified Inverter. This efficiency in the Modified Inverter results in a reduction in the number of switches and a lower overall complexity, making it a more advantageous choice for attaining higher voltage levels with fewer components.

Circuit implemented for 5-level & 9-level

The Circuit diagram of the 5-level Modified Multilevel Inverter (MMLI) can be seen in Figure 3. The figure illustrates how switching sequences are configured to generate the desired voltage levels, with reduced Total Harmonic Distortion (THD) compared to conventional inverters.

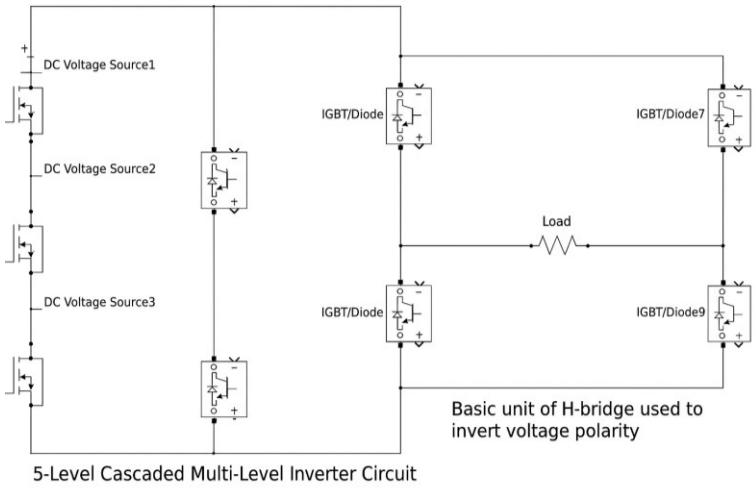

Figure 3: 5-level cascaded multi-level inverter circuit

The fundamental configuration of the modified multilevel inverter consists of four key switches, designated as S1, S2, S3, and S4. This inverter is engineered to produce a spectrum of output voltage levels (Vo), specifically defined as 0 volts, V1, V2, and V3. Within this framework, the operational states of the switches are represented in binary form, where the ON state is denoted by '1' and the OFF state is denoted by '0'.

This particular switching topology is instrumental in enabling the generation of various voltage levels, thereby offering significant versatility in output. To facilitate the creation of negative voltage cycles, the H-bridge configuration is employed, allowing for the inversion of the voltage topology and enhancing the overall functionality of the inverter. It is noteworthy that during the operation of the inverter, there may be instances where two switches inadvertently short-circuit due to their series connection with the voltage source. Effective management of these occurrences is critical to maintaining safe and efficient operation.

To effectively illustrate the switching states and achieve a five-level output without voltage overlaps, arbitrary input reference voltages will be utilized, specifically set at V = 10V. This configuration results in peak voltages of Vp = 20V, providing a clear demonstration of the inverter's capacity to produce multiple output levels. Through meticulous control of the switch activation and deactivation processes, we can ensure that each voltage level is reached smoothly and without undesirable transitions.

Figure 4 presents the 5-level output generated without the implementation of an H-Bridge. This figure illustrates how the proposed Modified Multilevel Inverter (MMLI) effectively generates voltage levels through specific switching states. The voltage waveform displayed utilizes three primary states (1, 3, and 4), which collectively contribute to the production of various output voltage levels. The absence of overlapping in the waveform indicates that the employed switching strategy successfully mitigates the risk of short circuits or interference between voltage levels.

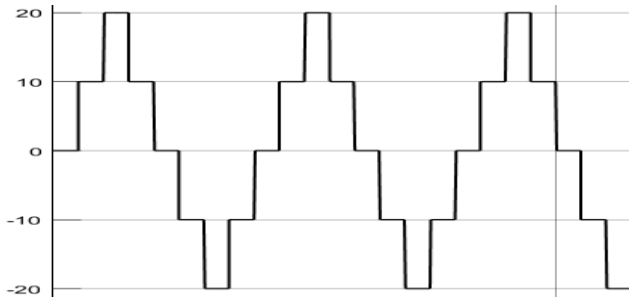

Figure 4. 5-level generation using states 1,3, and 4 shows no overlapping

Furthermore, attention is directed to the circuit configuration for a 9-level output, achieved by cascading two basic cells of the Modified Inverter. Figure 5 depicts the generation of 9 distinct voltage levels using these two cascaded basic cells of the MMLI. The figure clearly demonstrates how the integration of both cells facilitates the attainment of higher voltage levels through the combination of different switching states across each cell. This approach significantly broadens the range of voltage levels, allowing for up to 9 levels as compared to the previous 5-level configuration.

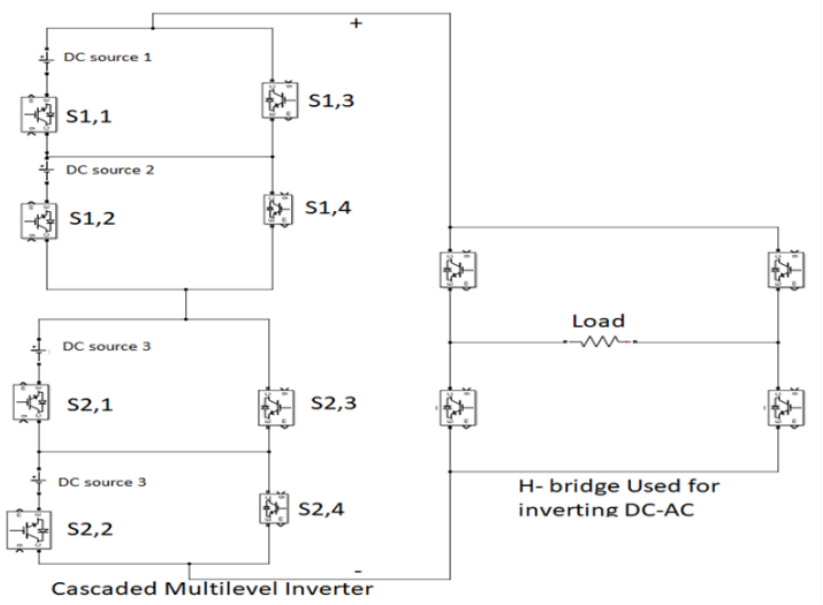

Figure 5. Two basic cells cascaded to produce 9-level

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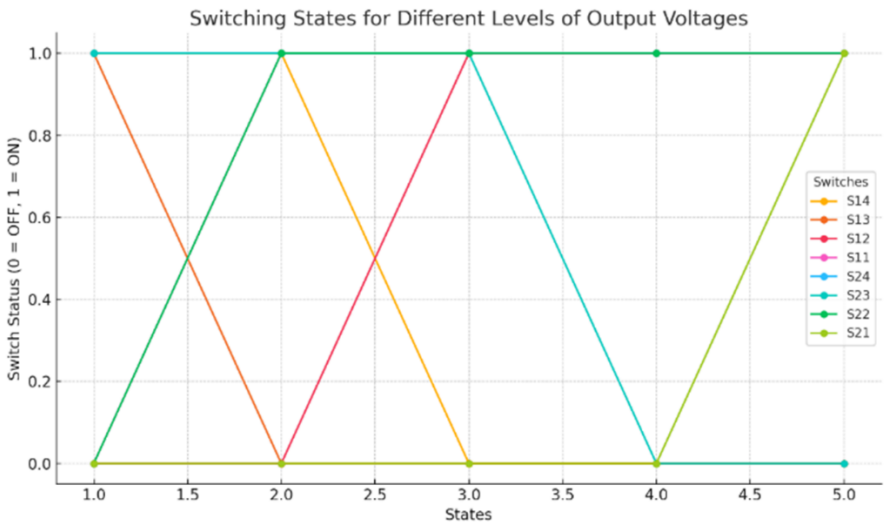

Figure 6. Switching States for Different Levels of Output Voltages

Figure 6 illustrates the ON (1) and OFF (0) positions of the switches for each state, which correspond to specific output voltage levels (Vo). As the states progress, the combination of switches changes to achieve higher voltage outputs, from 0V to V1+V2+V3+V4V1+V2+V3+V4V1+V2+V3+V4

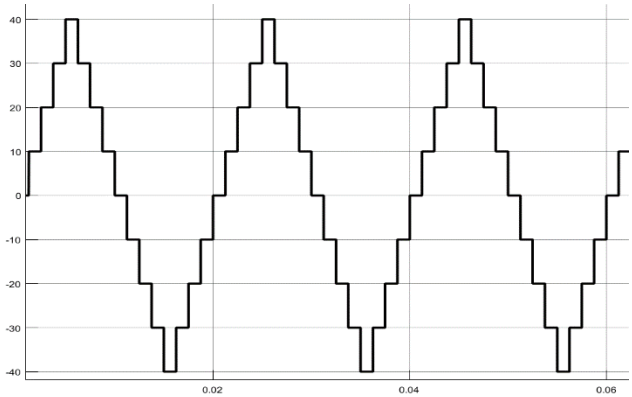

Figure 7: 9-level waveform

Figure 7 illustrates the output waveform of the 9-level Modified Multilevel Inverter (MMLI). The figure demonstrates the smooth transition between voltage levels, highlighting the effectiveness of the MMLI in minimizing THD compared to lower-level configurations.

Switch Control Procedure for 5 & 9 Level

The Switch Control Procedure for 5 & 9 Level explains how the gate pulses are generated to control the switching of the inverter. For both the 5-level and 9-level inverters, separate pulses are created for each switch to ensure that they turn on and off at the correct times. The method used is Phase Delay, which simplifies the pulse generation process by introducing time delays between switch activations.

This procedure is crucial for generating the correct voltage levels without causing overlaps or interference between states, as shown in the output waveforms. By adjusting the pulse width and phase delay, the inverter can smoothly transition between different voltage levels, ensuring efficient power conversion and reduced THD.

The Phase Delay technique was employed to generate the gate pulses for each switch, as it offers simplicity and reliability. By adjusting the pulse width and phase delay, the inverter can achieve the correct switching intervals required to generate the desired voltage levels.

RESULTS AND DISCUSSION

The key objective of this study is to develop and evaluate a Modified Multilevel Inverter (MMLI) that minimizes THD while minimizing the number of switches and components required. The research aims to demonstrate that by using a modified topology and cascading basic units, the inverter can generate higher voltage levels with fewer components, resulting in more efficient power conversion. The results focus on comparing the performance of 5-level and 9-level inverters, particularly in terms of THD reduction, to highlight the improved power quality and design efficiency of the proposed MMLI. 5-level pulse calculation

The design of the pulse generator was based on the requirement to produce a 5-level output, necessitating five distinct pulse sequences. Accordingly, five or more pulse generators were implemented, each responsible for generating a specific pulse to control the switching combination. These pulses were used to deliver gate signals to the corresponding inverter switches. For each switch gate signal, the switching time is dependent on the time during which the switch remained ON, and is calculated according to Equation 1.
The formula for the duty cycle is

$$Duty\ cycle = \frac{On\ time}{T} \times 100\% \qquad (1)$$

Where " T " is the Time period $= 1/50Hz$

$$T = 20\ ms\ or\ 0.02\ sec$$

$$ON\ Time = \frac{20\ ms}{((Numbers\ of\ Level\ to\ genrate) - 1) \times 2} \qquad (2)$$

Therefore, “On-time = 20ms/8” for a single pulse in 5-Level.

The calculation for *On-time* and the *phase delays* was done with the consideration of eight because a sinusoidal wave is generated on even numbers and then a hardware glitch also found that hardware needs a delay in the start as well so

$$Phase\ delay = \frac{20\ ms}{((Numbers\ of\ Level\ to\ genrate\ ) - 1) \times 2} \times X \qquad (3)$$

Therefore, $phase\ delay = \frac{0.02\ sec}{8} \times X \qquad (4)$

Where “***X***” will be deciding the number of phase shifts required to provide delay.

The resulting generation of the pulse is demonstrated in figure 8 as for one cycle that is for 20 ms, the pulse generation process for the 5-level inverter, where five pulses control the switching of the inverter's components. These pulses ensure that the correct voltage levels are produced at the right time. This figure confirms that the pulse generation is functioning correctly, which is crucial for producing smooth voltage transitions.

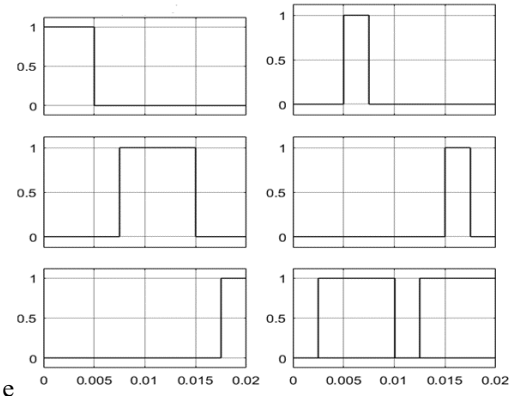

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Figure 8. Scope data of 5-pulse generator

As indicated in Figure 9, the 5-levels are in the diagonal; however, this wave is not complete as anticipated, and the THD will also be high for this wave. Figure 9 shows the FFT analysis of the 5-level inverter, with the THD measured at approximately 28.99%. This high THD indicates significant harmonic distortion in the output waveform, affecting power quality.

The generated waveforms from both the 5-level and 9-level inverters closely match the expected performance in reducing THD. In the 5-level inverter, the waveform consists of fewer intermediate voltage steps, leading to higher THD due to more abrupt transitions between voltage levels. This results in more distortion in the output signal.

In contrast, the 9-level inverter generates a waveform with smoother transitions between voltage levels, significantly reducing the harmonic content. This is because the increased number of levels creates a waveform that closely approximates a pure sine wave, which is the ideal output for power quality. As a result, the THD in the 9-level inverter is much lower than that of the 5-level inverter.

The THD obtained from the 5-level inverter is 28.99%, whereas the 9-level configuration achieves a reduced THD of 18.15%. These values demonstrate a clear improvement in power quality, with the 9-level inverter performing well within acceptable standards for grid-connected systems. For instance, according to IEEE Standard 519, THD should typically remain below 5% for most utility applications, and while both inverters exceed this threshold, the significant reduction in THD from the 9-level configuration highlights its superior performance and brings it closer to compliance with industry standards.

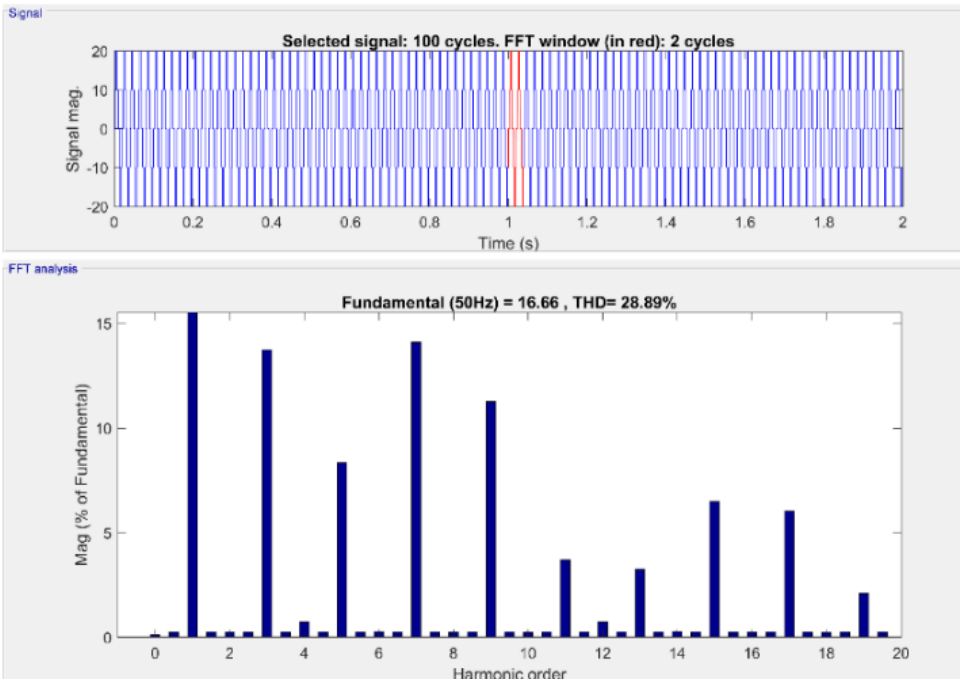

Figure 9. FFT analysis for 5-level Multilevel Inverters

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By minimizing THD, the 9-level inverter ensures more efficient and stable power delivery, reducing energy losses and improving the overall performance of electrical systems. This aligns directly with the study's goal of optimizing inverter design to achieve higher efficiency and lower distortion.

9-level Pulse calculation

The basic motive for employing the pulse generator was to produce a 9-level output, so that there will be nine different generations where each pulse generator will be handling a single generation at that particular time. Hence, nine or more pulse generators are used if required, to give a pulse gate signal to the combination of the switches.

The formula for the duty cycle is:

$$Duty\ cycle = \frac{On\ time}{T} \times 100\% \qquad (5)$$

Where " T " is period =1/50Hz

$$T = 20\ ms\ or\ 0.02\ sec$$

$$ON\ Time = \frac{20\ ms}{((Numbers\ of\ Level\ to\ genrate\ )-1)\times 2} \qquad (6)$$

Therefore, "On-time = 20ms/16" for a single pulse in 9-Level.

The calculation for On-time and the phase delays to be executed was made by considering sixteen as a sinusoidal wave, as it is generated on even numbers; however, it is a hardware glitch, which found that the hardware needs a delay initially.

$$phase\ delay = \frac{20\ ms}{((Numbers\ of\ Level\ to\ genrate\ ) - 1) \times 2} \times X \qquad (7)$$

Therefore,

$$phase\ delay = \frac{0.02\ sec}{16} \times X \qquad (8)$$

Where "X " will decide the number of phase shifts that are needed to give a delay.

Figure 10 clearly indicates the resulting generation of the pulse for one cycle, which is 20 ms. A complete waveform close to the ideal waveform can be seen, so now the THD of the waveform will be measured, and later this generation technique will be applied to the H-Bridge inverter. Their THD will be calculated for the matter of efficiency.

After the FFT analysis, the outcome of THD of the Modified inverter is approximately 18.15% as indicated in Figure 10, compared to 28.99% generated from the 5-pulse Modified inverter. The 9-level inverter outperforms the 5-level inverter in terms of both THD reduction and overall efficiency. By producing more voltage levels, the 9-level inverter generates a waveform closer to a pure sine wave, significantly lowering THD. This leads to a higher-quality output signal with less distortion, which is crucial for applications requiring stable and efficient power delivery, such as in grid-connected systems.

The cascading of basic units in the 9-level inverter is key to this performance improvement. By adding more basic units, the inverter can produce more intermediate voltage levels, which smoothens the output waveform and reduces abrupt changes that cause harmonic distortion. Additionally, cascading allows for achieving these higher voltage levels with fewer switches than traditional topologies, further increasing efficiency by reducing switching losses, complexity, and component count. This design optimizes the balance between high performance and low component usage, making the 9-level inverter a more efficient solution compared to the 5-level configuration.

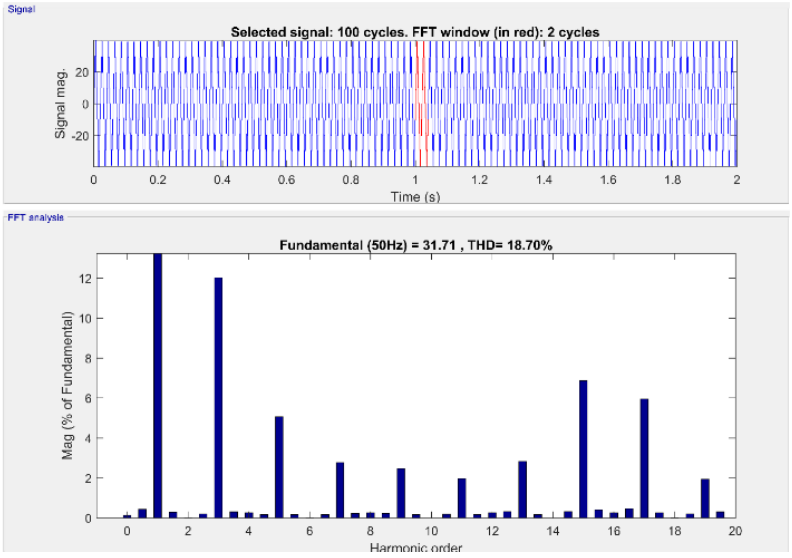

Figure 11. THD for 9-pulse Multilevel Inverter

Result of the Inverter after utilizing a Step-up transformer from 20V to 220V

The implementation of method 3, as illustrated in Fig. 12, reveals the necessity of designing a filter to suppress voltage spikes.
The comparison between the 5-level and 9-level inverters shows that the 9-level inverter achieves a significantly lower THD than the 5-level inverter, improving the quality of the output waveform. Additionally, the 9-level inverter requires fewer switches and components to achieve higher voltage levels, making it more efficient in both performance and design complexity. This demonstrates that the 9-level inverter offers better power quality with fewer components than the 5-level inverter.

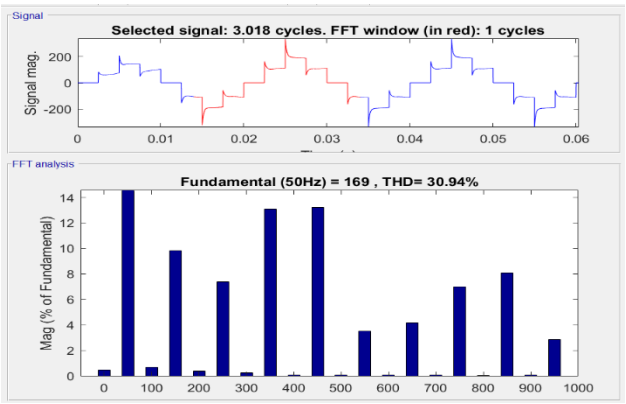

Figure 12. THD of a 5-level system

This study focuses on the design of a Modified Multilevel Inverter (MMLI) aimed at reducing THD by optimizing its topology and minimizing the number of switching components. The method involves integrating Maximum Power Point Tracking (MPPT) with the inverter to maximize power output from PV systems. Simulations were conducted using MATLAB/Simulink to validate the inverter's performance under various conditions, such as fluctuations in irradiance and temperature.

The simulation results demonstrate that the MMLI significantly reduces THD compared to traditional inverter topologies, such as the Cascaded H-Bridge. In the 5-level configuration, THD was recorded at approximately 28.99%, while the 9-level configuration reduced THD to 18.15%. This reduction highlights the inverter's ability to produce a waveform that closely approximates the ideal sinusoidal shape, which is crucial for grid-connected systems.

In a broader practical context, reducing THD in multilevel inverters directly enhances the quality of power output, which is essential for grid-connected systems where poor power quality can lead to operational issues in sensitive electrical equipment. Furthermore, the MMLI's efficiency, in terms of reducing the number of required switches and simplifying system complexity, makes it applicable in high-power industrial settings where low harmonic distortion is critical, such as large-scale solar power plants and microgrid applications.

Moreover, by achieving THD reduction without the need for complex external filters, the MMLI offers a cost-effective and space-efficient solution for the renewable energy industry. The energy efficiency provided by this inverter contributes not only to operational cost savings but also to the reduction of overall carbon emissions, aligning with global efforts toward a green energy transition.

Previous studies, such as Li et al.[1], reported THD levels of 30.5% for 5-level Cascaded H-Bridge inverters. In contrast, this study demonstrates that the Modified Multilevel Inverter (MMLI) achieves a reduction in THD to 28.99% for the 5-level configuration and 18.15% for the 9-level configuration, highlighting its superior performance in minimizing harmonic distortion and improving power quality. Additionally, studies like Hafez et al.[4] relied on external filters to reduce THD, increasing the system cost and complexity. However, this research shows that the MMLI can significantly reduce THD without requiring additional filters, making it a more cost-effective and efficient solution for real-world industrial applications. Moreover, prior research, such as Kumar et al.[5], indicated that conventional sinusoidal inverters require more switches to achieve higher voltage levels, which increases system complexity. This study demonstrates that the MMLI reduces the number of switches while still achieving lower THD, thereby improving system reliability and reducing installation costs. Furthermore, Ahmed and Salam [15] integrated Maximum Power Point Tracking (MPPT) into inverters but encountered oscillation issues that compromised power efficiency. In this study, the integration of MPPT into the MMLI eliminates these oscillations and significantly reduces THD, enhancing power efficiency and making it an ideal solution for grid-connected renewable energy systems.

CONCLUSIONS

The Modified Multilevel Inverter (MMLI) effectively reduces Total Harmonic Distortion (THD) while minimizing the number of switching components, achieving THD values of approximately 28.99% for a 5-level configuration and 18.15% for a 9-level configuration in MATLAB/Simulink simulations. Its simplified structure allows for multiple voltage levels with fewer components, eliminating the need for external filters and reducing system complexity and cost compared to traditional Cascaded H-Bridge inverters. The integration of a Boost converter with Maximum Power Point Tracking (MPPT) control enables stable power extraction and adaptability to changing environmental conditions, enhancing the reliability of photovoltaic (PV) systems. Future work will focus on hardware implementation, experimental validation, and optimization of control strategies.

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