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Design and Simulation of a QPSK Demodulator Using Discrete Components

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A B S T R A C T

Quadrature Phase Shift Keying (QPSK) is a widely adopted digital modulation technique that encodes two bits of information in each symbol by utilizing four distinct phase states separated by 90 degrees. This approach offers high spectral efficiency, making it especially suitable for modern communication systems that demand robust data transmission with limited bandwidth. This investigation details the design process and LTspice-based simulation of a QPSK demodulator constructed entirely from discrete electronic components. This work addresses a gap in previous research, which has largely relied on integrated circuits or software-based algorithms, by focusing on circuit-level implementation using basic analog and digital components. The demodulator was assembled on a prototype PCB, combining fundamental operational amplifiers, mixers, filters, and digital logic gates to perform the required signal processing functions. The evaluation involved testing the demodulator's ability to accurately recover the transmitted data and its operational stability. Simulation results demonstrated reliable performance across all stages, with the demodulator successfully maintaining phase detection accuracy and reconstructing the original 8-bit test sequence with high fidelity. Under test conditions with a 1 MHz carrier frequency and a data transmission rate of 500 kHz, the recovered signal showed an approximate delay of 4.5 microseconds attributable to the sequential parallel-to-serial conversion process. Despite the delay, the demodulator maintained full symbol-level correlation with the transmitted data stream. These findings confirm that a discrete component-based QPSK demodulator can effectively support reliable digital communication, highlighting its practicality for educational purposes, low-cost prototyping, laboratory training, and preliminary hardware development in the field of wireless and wired communication systems.

INTRODUCTION

Digital modulation technologies have advanced further in the current digital era, providing increased efficiency and greater practicality. Quality, flexibility, and dependability have significantly improved as communication systems have developed, especially in the field of digital modulation [1]. For digital information to be transmitted effectively over analog channels, digital modulation is a fundamental process in telecommunications. Discrete digital signals are embedded onto a continuous analog carrier wave using this technique. Amplitude Shift Keying (ASK), which modifies the carrier's amplitude; Frequency Shift Keying (FSK), which modifies its frequency; and Phase Shift Keying (PSK), which modifies its phase, are the primary techniques used to accomplish this transformation. In order to enable reliable and spectrally efficient data transmission in contemporary communication systems, these fundamental digital modulation schemes are essential [2].

An improved version of PSK, called Quadrature Phase Shift Keying (QPSK), applies specific phase shifts to the carrier signal to encode two bits per symbol. This technique works by dividing the input data stream into even and odd bits, each mapped onto one of four phase states: 0°, 90°, 180°, or 270° [3].

In digital communication systems, the modulator and demodulator, collectively referred to as a modem, are essential parts. Assuring precise and dependable data recovery at the receiver end, the demodulator extracts the original message from the received modulated signal after the modulator encodes the information signal onto a carrier wave for effective transmission [4].

Although extensive work has been accomplished in the design and implementation of the QPSK modulator, the associated demodulator design has received less attention. Various research studies [5], [6], [7] have successfully accomplished the design of the QPSK modulator, in which integrated circuits (ICs) or Field Programmable Gate Arrays (FPGAs) are used. The use of ICs and FPGAs may prove to be quite expensive, particularly during the

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development stages. Moreover, another cost-effective and educational choice could be the use of discrete devices, which can be easily acquired and are also a reliable option for small applications [2], [8].

Moreover, simulation software such as MATLAB has been widely utilized in the assessment of designed QPSK systems in controlled conditions, shedding light on the creation of signals [9], [10], [11]. Nonetheless, simulation has primarily focused on the design of the modulator, while the demodulator has remained less explored, especially in the context of discrete component implementations. This has resulted in a lack of understanding of the potential of an entire QPSK modem, which contains both the modulator and the demodulator, in discrete component implementations.

The current study fills this gap by presenting a comprehensive QPSK modem design that uses only discrete electronic components to implement the modulator and a recently created demodulator section. In addition to designing the demodulator, this study assesses the viability of the demodulator's performance for hardware implementation by determining how well it simulates real-world conditions prior to physical hardware implementation.

For this study, the LTspice simulation platform was selected due to its high modeling accuracy for analog and mixed-signal circuits, its effectiveness in frequency and transient domain analysis, and its adaptability in assessing the behavior of discrete components. Due to these characteristics, LTspice is particularly well-suited for verifying circuit-level performance and ensuring the demodulator functions properly prior to hardware implementation. This research has substantial pedagogical value in addition to its practical value, as the resulting QPSK output signals are easily analyzed and comprehended, making them ideal for educational settings.

There are four sections in this paper. The study's background and motivation are presented in Section I, which also highlights the development of QPSK modulation and its uses. The design and simulation procedure of the QPSK demodulator in LTspice, including setup, calibration, and methodology for ensuring reproducibility, is described in Section II. The simulation results are presented in Section III, along with a quantitative comparison to earlier studies and a discussion of the performance of the designed demodulator. The paper is finally concluded in Section IV, which also offers some possible avenues for further research, such as the physical implementation of the suggested demodulator and its use in actual communication systems.

METHODS

The flowchart illustrates the simulation process for analyzing the performance of the QPSK Demodulator in the LTspice simulation tool. The simulation process in this research involves a series of sequential tasks, as described in the flowchart in Figure 1, which outlines the simulation process. First, there is the creation of the 8-bit test sequence, which is the binary code ‘11011000’. This code serves as the input data for analyzing the demodulation process. The binary code ‘11011000’ has been segmented into two other binary codes that run in parallel to form the I-channel and Q-channel signals, as the binary code must comply with the mapping format in the QPSK process.

After the data for the test has been prepared, the simulation environment in LTspice can be set up by specifying the most important parameters of the circuit, like the carrier frequency set to 1 MHz, the data rate of 500 kHz, as well as the specifications for the oscillator, the filters, among others, in the circuit. After this, the simulation can be performed in the time domain.

The outputs from the mixing process are extracted to produce the I and Q baseband signals. These signals are then filtered through low-pass filters to eliminate the remaining high-frequency content, thereby extracting the desired baseband information. The process of bit regeneration then occurs through the use of decision logic based on thresholds, converting the filtered analog signals back into binary bits.

The clock recovery function ensures the necessary timing alignment of the symbols before the regenerated I and Q bits are processed in a parallel-to-serial conversion stage, producing a single, reconstructed output stream. The process ends with the verification step, in which the output sequence is verified against the original input sequence to ensure the correctness of the process.

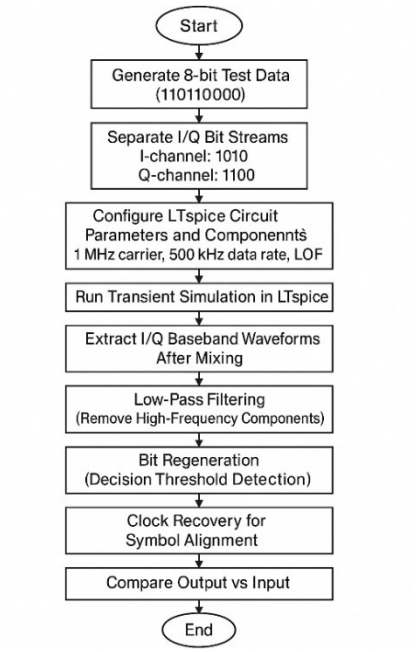

Figure 1. Flowchart of the Simulation Procedure for the QPSK Demodulator

Designing a QPSK Demodulator

The structure of the Quadrature Phase Shift Keying (QPSK) Demodulator, as shown in Figure 2, comprises several key functional blocks essential for the successful recovery of the digital information transmitted. These key functional blocks include the reception stage of the QPSK, the multipliers for the down conversion process, the LPF used in the baseband recovery, the bit regenerators for the decision process from the analog to the digital format, the clock recovery circuit, as well as the P/S circuit for the reconstruction of the data output.

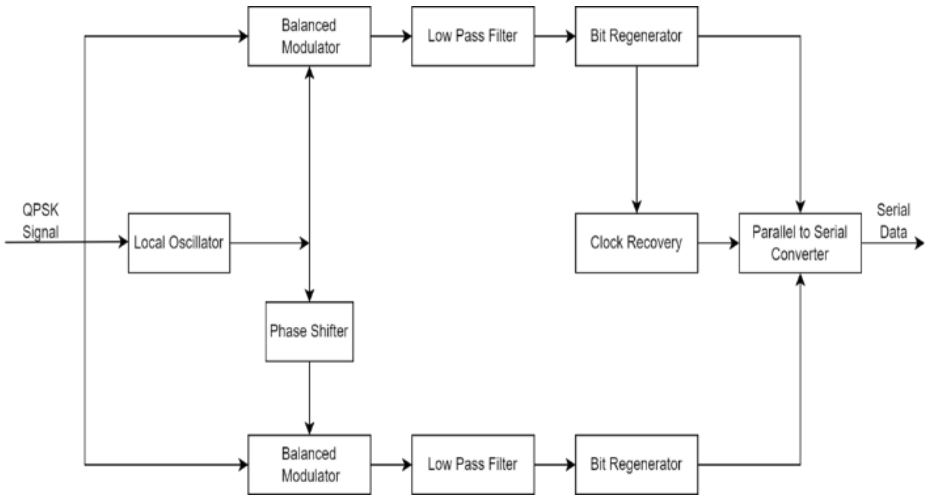

Figure 2. Block Diagram of the Main Processing Stages in the QPSK Demodulator [3]

Each block plays a specific and essential role in the demodulation process. The signal multipliers are responsible for converting the received QPSK signal to baseband, achieved by coherently multiplying the incoming signal with in-phase (0°) and quadrature-phase (90°) components derived from local carrier signals. Following this, the signals pass through low-pass filters (LPFs), which serve to eliminate high-frequency noise and undesired spectral components while maintaining the integrity of the baseband I (In-phase) and Q (Quadrature-phase) signals. These filtered analog signals are then fed into bit regenerators, which accurately convert the analog waveforms into binary levels, preparing them for digital processing. The clock recovery block is crucial for generating precise timing signals, which enable proper sampling of each bit and ensure synchronization with the transmitted data. Finally, the separated I and Q bit streams are combined and converted into a serial output sequence, providing the demodulated data stream for further processing or decoding.

To support the reproducibility and independent verification of the proposed QPSK demodulator, Table 1 provides a summary of all the main electrical features and circuit components. The MC1496 balanced modulator, operational amplifier stages, Sallen-Key filter components, logic devices, and supporting resistive capacitive networks are among the active and passive components whose crucial parameters are consolidated in the table to guarantee that every functional block can be accurately reconstructed. Component tolerances, supply voltage levels, gain settings, and cutoff frequency-defining elements are all explicitly specified in this specification, making it useful for both implementing the design on real hardware and reproducing the LTspice simulation environment. Such thorough documentation enhances the reproducibility of the demodulation architecture for ongoing research and educational use, permits direct comparison with future implementations, and promotes methodological transparency.

Table 1. Component Specifications Used in the QPSK Demodulator

Component	Model	Key Specificatios	Purpose in Circuit
Balanced Modulator	MC1496 [12]	Operating freq. 0–50 MHz, differential inputs, adjustable carrier nulling	Down conversion of received QPSK signal into I/Q baseband signals
Phase Shifter (90°)	RC All pass network [13]	Phase shift ≈ 90° at 1 MHz, minimal amplitude attenuation	Generates quadrature carrier reference for I/Q separation
Local Oscillator	Sine wave source [14]	1 MHz carrier, 1–2 V amplitude, stable frequency	Provides reference carrier for coherent detection
Op-Amp	LM358 [15]	Dual op-amp	Filtering, signal amplification, and threshold decision stage
Low Pass Filter (LPF)	Sixth Order Sallen Key Low Pass Filter [16]	Cutoff frequency at 0.5 MHz (half of the 1 MHz carrier)	Extracts baseband I/Q signals after mixing
Bit Regenerator	Op-Amp Comparator [17]	TTL compatible output, fast switching, adjustable threshold	Converts baseband analog signals into digital binary outputs
Clock Recovery Circuit	MC74HC4046 [18]	Lock range 1–10 MHz, built-in phase comparator	Recovers timing reference for symbol alignment
Parallel to Serial Converter	Logic gates [19]	Two D flip-flops, two AND gates, and one OR gate, which together produce a serial data output	Merges I/Q output bits into serial data stream

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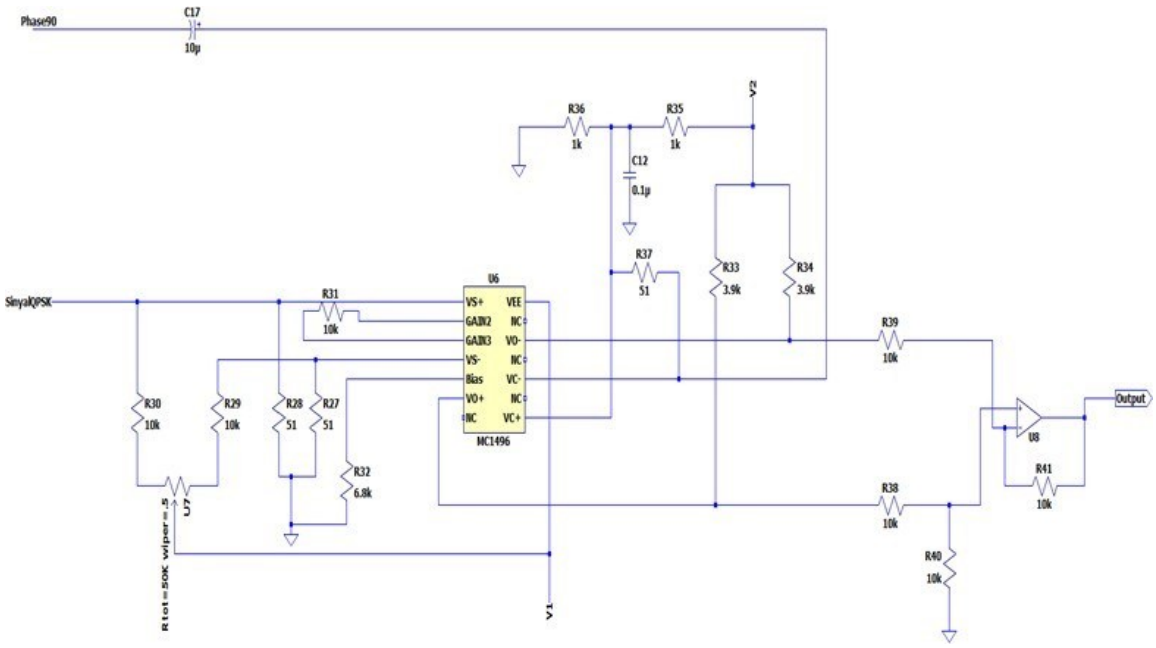

Figure 3. MC1496 Balanced Modulator Circuit Implemented for Coherent I/Q Signal Extraction [12]

Balanced Modulator Circuit

The balanced modulator used in the demodulation stage functions as the core element for multiplying the incoming QPSK signal with the carrier signal. For the simulation, it was assumed that the modulated information was transmitted from the modulator to the demodulator through a wired link. The process involves the use of the MC1496 chip, designed as indicated in the manufacturer's recommendation, through the supplementary use of the differential amplifier, as indicated in Figure 3 [12]. Operating with two primary inputs, the received QPSK waveform and the coherent carrier signal, the MC1496 produces a baseband information signal that is subsequently passed through a low-pass filter for further processing. The balanced modulator requires the coherent process, performed through the use of the in-phase carrier, along with the quadrature carrier, as indicated in the cosine and sine functions, to effectively convert the QPSK to the embedded information [3].

In order to unlock the desired baseband signals, the result obtained from the balanced modulator needs to be filtered using an LPF, attenuating the undesired high-frequency information produced as a result of the modulation process [20]. This particular step also helps ensure that the resulting I/Q signals accurately represent the original information bits.

Low Pass Filter Circuit

The low-pass filter (LPF) essentially targets the propagation of the signal aspects whose frequencies are below a specified cutoff frequency, while simultaneously suppressing all frequencies in excess of the specified threshold [16]. This key objective remains indispensable in distinguishing the desired baseband signals from the interference signals in the higher frequency bands, as depicted in Figure 4. For optimal QPSK demodulation operation, the cutoff frequency is tuned to half the carrier frequency. This approach takes into consideration the centrosymmetric spectral representation of the modulated signal in the frequency domain, centered at the carrier frequency. The placement of the cutoff frequency at 0.5 MHz, which represents half the carrier frequency of 1 MHz, enables the filtering operation to distinctly pass the desired signals while suppressing the presence of noise in the higher frequency bands [16], [21].

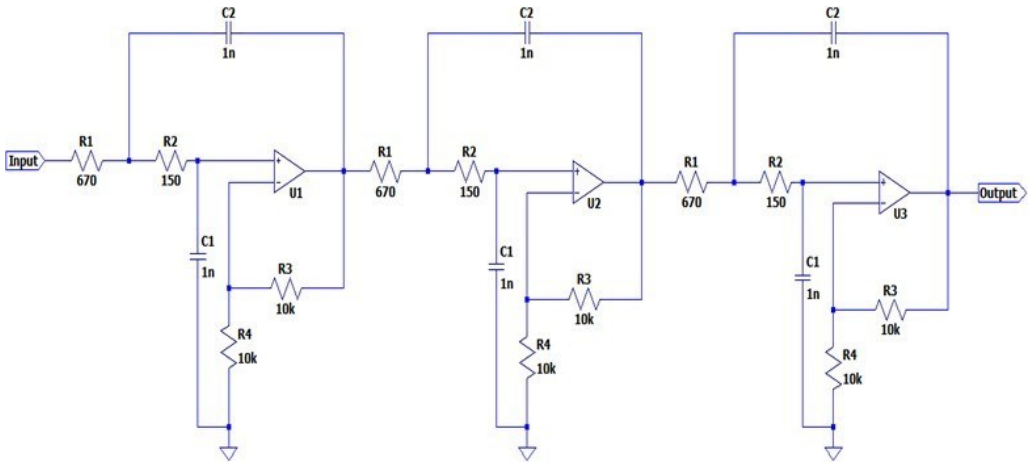

Figure 4. Sixth Order Sallen Key Low Pass Filter Circuit for Baseband Signal Extraction [7]

This approach corresponds to the spectrum of the QPSK signals, as the baseband information in these signals resides symmetrically around the carrier. The deliberate placement of the cut-off frequency at this particular midpoint also plays a crucial role in the proper functioning of the low-pass filter [22]. This particular arrangement helps in the seamless transfer of the desired baseband information in the low frequency region, which possesses the crucial information signal, while simultaneously enabling the effective attenuation of the undesired harmonic entities in the form of noise, which are inevitably produced in the process of modulation as well as demodulation [23].

Bit Regenerator Circuit

The bit regenerator circuit plays a crucial role in the demodulation process by converting the analog output signal from the low-pass filter (LPF) back into discrete digital bits [24]. As illustrated in the circuit diagram in Figure 5, this circuit primarily consists of an operational amplifier (Op-Amp) configured as an inverting comparator, followed by an X-NOR gate.

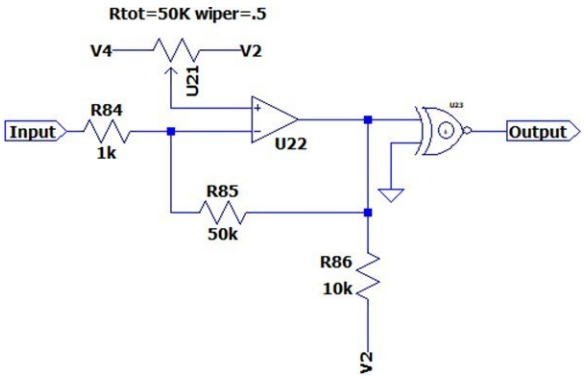

Figure 5. Bit Regeneration Circuit Used To Convert Filtered Analog Waveforms Into Digital Outputs

In this implementation, the Op-Amp is operated in an inverting configuration, producing an output that is 180° out of phase with the input signal. The gain of the comparator stage is selected based on typical design practices for QPSK demodulators, where an amplification factor between 30 and 50 is commonly used to ensure appropriate signal swing and threshold sensitivity [24]. Accordingly, a gain value of 50 was adopted for this design to establish a well-defined analog-to-digital decision boundary. This configuration enables the comparator to generate a stable binary output that is subsequently processed by the X-NOR logic stage [25].

Clock Recovery Circuit

The clock recovery process involves the use of a set of circuits, which comprises a Phase-Locked Loop (PLL) designed using the MC74HC4046 chip [18] and a D flip-flop, as depicted in Figure 6. The choice of the MC74HC4046 chip was based on its low power dissipation and stability at high frequencies, which allows for an uninterrupted clock output signal during the synchronization process. In the clock recovery circuit design, none of the values of the PLL circuit, designed using the MC74HC4046 chip, were altered to accommodate the needs of the proposed QPSK demodulator in this research. This was done in order to ensure the stability of the output clock signal produced by the designed circuit. The PLL in the MC74HC4046 chip has properties well-suited to the needs of this research, as it can synchronize the output signal's frequency to that of the incoming signal in an automatic process, ensuring that the frequency of the output signal equals that of the incoming signal [26].

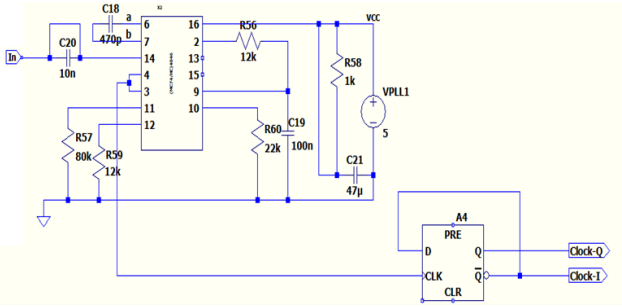

Figure 6. PLL-Based Clock Recovery Circuit Designed To Synchronize Symbol Timing

Parallel to Serial Converter Circuit

The parallel-to-serial converter circuit is designed to transform two parallel bit streams into a single serial output sequence. As shown in Figure 7, the circuit comprises two D flip-flops, two AND gates, and one OR gate, configured to route the regenerated I and Q bits according to the recovered clock signal. In this configuration, the AND gate outputs a logic high (1) only when all of its inputs are at logic high, whereas the OR gate outputs a logic high (1) for any input combination except when all inputs are at logic low [19]. The D flip-flops operate as temporary storage elements that synchronize the parallel inputs before they are combined by the AND and OR logic stages.

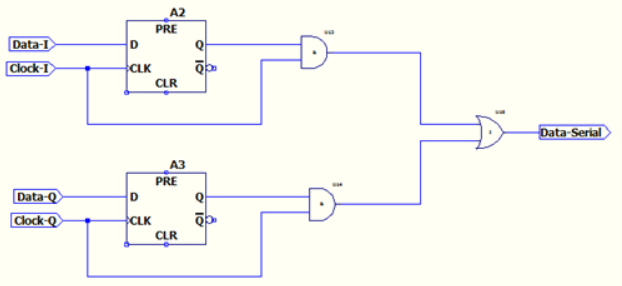

Figure 7. Parallel-to-Serial Converter Circuit for Combining Regenerated I/Q Bits Into Serial Data [27]

Through this arrangement, the circuit organizes the demodulated I and Q data into a serial bit stream suitable for subsequent digital processing stages. The use of standard logic gates and D flip-flops ensures predictable timing behavior and straightforward hardware implementation within the overall QPSK demodulation architecture [28].

RESULTS AND DISCUSSION

After completing the design of the QPSK demodulator, it was essential to conduct a simulation to validate the operation of the respective blocks, as well as the entire system. The simulation results obtained can be used to evaluate whether the designed demodulator was successful in generating the desired baseband signals, as well as the allocation of symbols in the I channel and the Q channel. On the other hand, the simulation process can help in the provision of some key values pertaining to the bit level as well as the timing delay, allowing the comparison of the efforts made in the project to the efforts made in the past, as reported in

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the literature, concerning discrete component designs of the QPSK model.

The simulation was conducted using LTspice, which offers high accuracy in both the time and frequency domains, making it suitable for discrete simulation of QPSK demodulators. In order to make the accuracy level of the simulation process as high as possible, the parameters involved in the simulation process, the model parameters of the balanced modulator made up of the MC1496 chip, the parameters involved in the Sallen-Key filter, as well as the parameters involved in the model illustrating the logical levels, were all specified as indicated by the manufacturer before the simulation process. The simulation flow chart, which explains the process involved in generating the data, configuring the circuit, and verifying the simulation result, is shown in Figure 1.

The demodulation process was examined using the 8-bit test pattern '11011000', chosen based on the transitions involved in the binary logical pattern, which facilitated the evaluation of phase detection under varied symbol conditions. In simulating the process involved in the various stages of demodulation, a carrier frequency of 1 MHz, along with a data rate of 500 kHz, has been considered, as this represents the standardized operating conditions for the entire process.

Balanced Modulator Result

The balanced modulator acts as the first stage in the demodulation process, where the received QPSK-modulated signal is coherently multiplied by the in-phase (0°) and quadrature-phase (90°) signals. The coherent multiplication process translates the modulated signal to its baseband, yielding the in-phase (I) and quadrature-phase (Q) signals, which carry the embedded information in digital form. This process is illustrated in Figure 8, which displays the in-phase and quadrature signals generated by the simulation in the LTspice platform. In this case, the I- and Q-channel signals exhibit the proper transitions in terms of the values related to the binary sequence '11011000', which was segmented into the binary sequences '1010' for the I-channel process and the '1100' sequence for the Q-channel process.

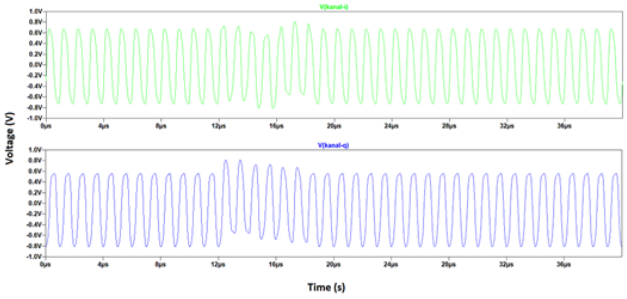

Figure 8. Output Signals of the I and Q Channels in the Balanced Modulator

The result obtained from the simulation in the balanced-modulator stage, using the LTspice tool, produced a clean I and Q baseband signal, as shown in Figure 8. The peak values measured in the I & Q channels were roughly 0.80V and 0.78V, respectively, with an amplitude variation reported at 2.5%. The baseband frequency extracted from the I & Q channel was, as expected, at 500 kHz, considering the original frequency to be 1 MHz.

The result obtained from the level verification of the symbol showed that there were no errors in the first 8 out of the 8 received symbols, thereby proving the efficiency of the multiplier, 'MC1496', in the process of synchronizing the carrier as well as the process of down conversion of the received signals [12].

In summary, these numerical results demonstrate that the balanced modulator stage has successfully generated baseband signals with minimal amplitude errors and accurate timing, thereby establishing a stable foundation for the subsequent LPF stages and bit regeneration stages.

Low Pass Filter Result

The low-pass filter (LPF) stage is responsible for extracting the baseband components produced by the balanced modulator by attenuating high-frequency mixing products. In this design, the LPF was configured with a 0.5 MHz cutoff frequency, corresponding to half of the 1 MHz carrier, to ensure that only the information-bearing components remain within the passband. Figure 9 shows the filtered outputs for the in-phase (I) and quadrature (Q) channels. The resulting waveforms exhibit the expected Butterworth behavior, characterized by a maximally flat passband and a smooth, monotonic roll-off beyond the cutoff frequency. This response effectively reduces the residual carrier components while preserving the amplitude transitions required for symbol recovery [16].

According to the frequency domain response, the filter attenuates by approximately −3 dB at the 0.5 MHz cutoff, preserving in-band components while suppressing higher-frequency harmonics more effectively. The LPF generates clean baseband waveforms suitable for precise bit regeneration, as evidenced by the consistent amplitude levels and distinct symbol boundaries of the filtered I and Q signals.

These results validate that the LPF exhibits consistent and predictable filtering performance, yielding minimally distorted baseband signals and providing the signal integrity required for dependable operation in subsequent demodulation stages.

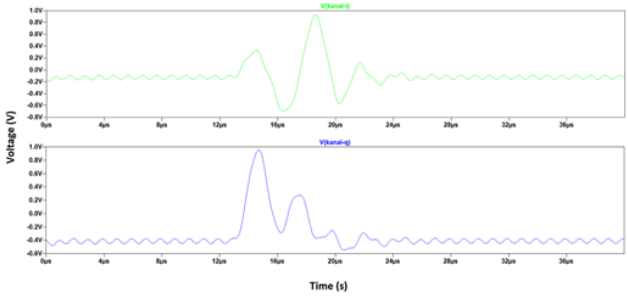

Figure 9. Output Signals in the I and Q Channels

Bit Regenerator Result

Following low-pass filtering, the analog baseband signals were processed by the bit-regenerator circuit to restore their corresponding digital levels. As shown in Figure 11, the regenerator produced square-wave outputs that match the expected odd-bit (I-channel) sequence 1010 and even-bit (Q-

channel) sequence 1100, exhibiting clear and well-defined logic transitions.

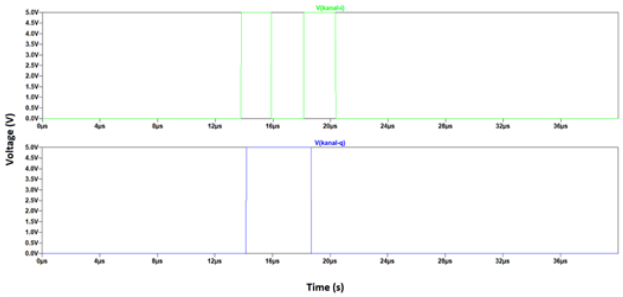

Figure 1. Bit Regenerator Output Signals in the I and Q Channels

The eight examined symbols were all successfully recreated, and no misinterpretation was detected in the simulated period, as verified at the symbol level. Furthermore, the recreated pulses exhibited stable transition times, which varied slightly from the 2μs period set for the transition time in the demodulation test. This confirms that the time alignment of the recreated bits was correct, as well as the functioning of the decision thresholds.

The regenerated digital bit streams produced in this manner are used to create the necessary intermediate outputs during the data reconstruction process. The accurate reconstruction of the data sent becomes possible by combining the I/Q-channel data with the recovered clock in the parallel-to-serial converter.

Clock Recovery Result

The clock recovery circuit generated the necessary two periodic timing signals for the synchronizing process of the I/Q-channel demodulated data streams. This was verified by the stable square-wave form of the recovered clocks, as shown in Figure 11, with a period of approximately 2 μs, as expected for the 500 kHz timing reference.

These restored Clock-I and Clock-Q signals operate in a steady manner, maintaining a complementary phase relationship where one clock is always in the low state while the other is in the high state. This complementary operation continues throughout the simulation period, thus ensuring the sampling of the I and Q data signals at non-overlapping times.

The equal spacing between the transitions in the clock signals indicates that the timing signals are in proper sync, which is a necessary requirement for the correct functioning of the parallel-to-serial converter.

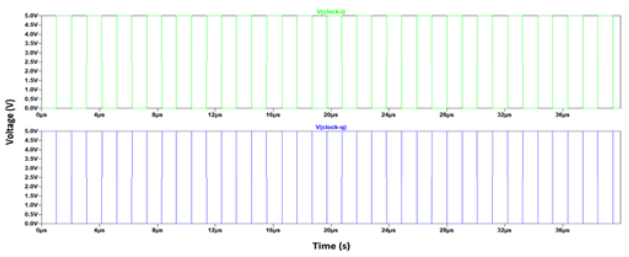

Figure 2. Clock Recovery Output Signals in the I and Q Channels

The top trace corresponds to the Clock Q signal, which is in green, while the lower trace corresponds to the Clock I signal, which is in blue. From the figure, it can be observed that the Clock I and Clock Q signals are logical complements of each other, where the clocks are in opposite logical levels, either at the logical high level or at the logical low level. This helps achieve time division control over the other two channels, allowing data from only one channel to be processed.

The circuit in the parallel-to-serial converter uses the recovered clock signals as the timing reference inputs. The D-type flip-flop in the parallel-to-serial converter is triggered by each clock, enabling the selective and sequential loading of data in the I and Q channels. The original bitstream, which was previously split and modulated in the QPSK process, is restored by alternately switching the pulses of the clocks, ensuring the proper temporal ordering of the I and Q data bits.

Parallel to Serial Converter Result

The last step in the demodulation process is where the original bitstream sequence is derived from the I/Q-channel outputs. The chosen 8-bit sequence for the experiment (11011000) involves deriving the odd bit sequence (1010) and the even bit sequence (1100) as inputs to the converter. The process involves the use of the converted clock signals, where only one channel can be sampled while the clock transitions.

The complete 8-bit sequence was successfully converted by the parallel-to-serial converter, as shown in Figure 11. The verification process at the symbol level confirmed the regeneration of the complete set of 8 bits in the correct time order. The demodulator successfully reassembled the received data in the correct format, as confirmed by the matching of the serialized output (waveform) of the process, which corresponds to the original binary stream used in the modulation process.

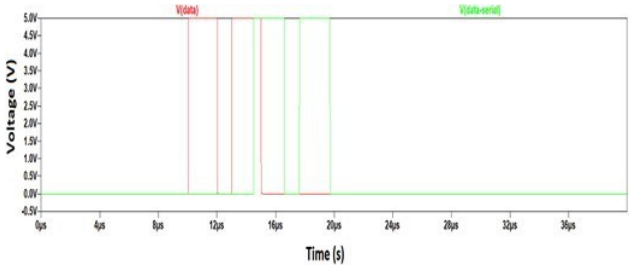

Figure 3. Input Data Signal and Demodulator Output Signal

There was a noticeable delay of around 4.5 microseconds between the regeneration of the parallel data and the final generation of the serial data. This period represents the inherent timing required for the alternating sampling of the I/Q signals, as well as the sequential loading of symbols in the converter. The serial data stream, although affected by this delay, remained fully consistent with the expected bitstream pattern, without any errant bits, throughout the sampling period.

These results demonstrate the successful operation of the parallel-to-serial converter, ensuring that the correct symbols are aligned and completing the QPSK demodulation process. The straightforward complexity of the designed logic structure, along with stable timing, indicates that this particular circuit should

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function well in both hardware and classroom applications in digital communication systems.

Discussion

In recent research work on QPSK demodulators, the emphasis has mainly been directed toward high speed, noise resistance, and integration density achieved using modern designs, such as synchronous CMOS receivers, systems for wideband acquisition, or loop-based carrier recovery. For example, in the work described in [29], the CMOS QPSK receiver operating at a speed of 32 Gb/s provides excellent results for coherent demodulation based on heavily integrated analog frontend designs, while the wideband acquisition scheme proposed in [3] improves the range of carrier detection based upon integrated mixed-signal processing. Finally, in similar loop-based designs described in [30] and [31] there has been good noise resistance, along with sufficient phase locking, but rather involved management concerning loop filtering, the VCO, as well as the associated synchronization.

On the other hand, software-only efforts like the GUI-driven QPSK simulator described in [32] Supports conceptual learning, but lacks simulation of non-ideal analog issues, such as ripple, DC offset, filter distortion, and delay. Finally, the modular/modulator architecture described in [33]Although versatile in terms of the range of modulation schemes it can support, it lacks sufficient transistor-level details to make it ideal as a platform in the educational domain.

By employing the fully discrete component open loop architecture based purely upon just the balanced modulator chip MC1496, the sixth-order Sallen-Key low-pass filter, and simplified digital logic, the design for the demodulator presented in this work has a radically different approach to other designs, as it provides insight into the transitions happening at the baseband level at every stage of the way in the process of performing the demodulation. Verification at the symbolic level confirmed that the simulation corresponded to the full serialization of the original 8-bit information, along with the correct replication of the I/Q bit sequence.

One important quantifiable result involves the measured reconstruction time of 4.5 μs, which is significantly lower than the reported values of 5-12 μs in the PLL-based analog systems described in [30] and [31]. This has been made possible by eliminating the loop-based synchronizer and adopting deterministic down-conversion techniques. Although the proposed approach has not been designed to operate in the domain of extreme bands in the case of CMOS receivers [29], as well as in the domain of SNR in the case of wideband systems [3]It can be very effective in reducing circuit complexity in moderate-frequency communication modules, lab setups, and educational hardware.

Future work could include the use of lightweight synchronization techniques, for example, reduced complexity Costas loop designs, in order to assess the potential benefit in noise resilience as opposed to loop-based designs in [30] and [31]. The development of a hardware prototype could also facilitate the assessment of practical, real-world non-ideal behavior in relation to discrete component demodulator design, thereby allowing a fair comparison between the proposed architecture, the existing mixed-signal, as well as the existing analog designs in [3] and [33]. The exploration of the suitability of the design at increased carrier frequencies can also help shed light upon the scalability boundaries of discrete component demodulator designs in relation to existing CMOS-based, high-speed receivers in [29]. These developments would extend the practical applicability of the proposed architecture while retaining its defining advantages of simplicity, transparency, and ease of implementation.

CONCLUSIONS

In this research, a discrete component QPSK demodulator was designed and simulated using the LTspice Simulator to examine the feasibility of its hardware implementation. The simulation outputs confirmed the successful decoding of the transmitted binary information after a time delay of 4.5 μs, indicating a high level of synchronization between the original and reconstructed signals in the presence of a carrier frequency of 1 MHz and a data rate of 500 kHz. These simulation outputs confirm the validity of using discrete components in detecting phase information and reconstructing the QPSK signal.

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